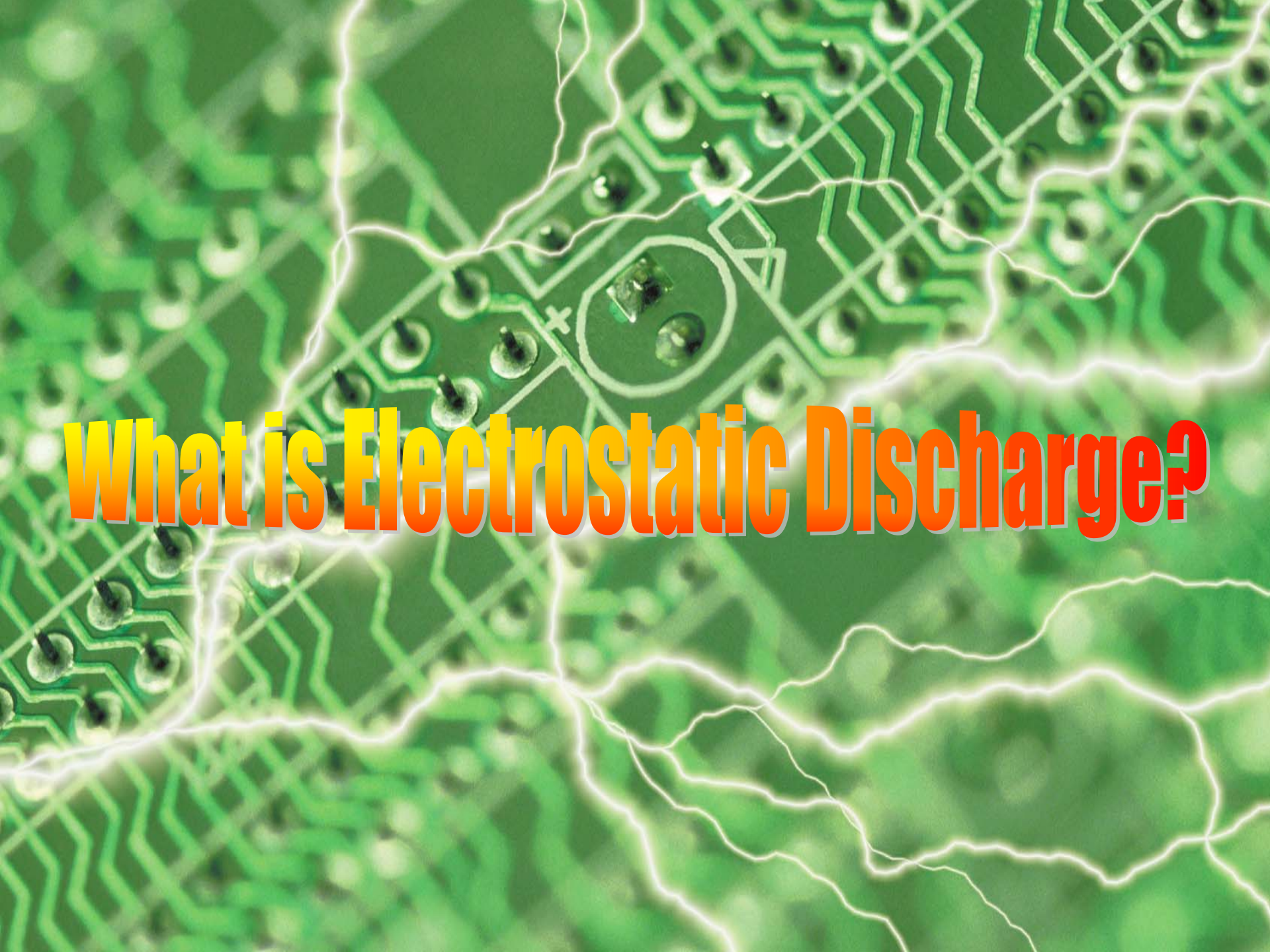
Electrostatic Protection for Semiconductor Electronics

Charvaka Duvvury

Silicon Technology Development

Texas Instruments Inc., Dallas, Texas, USA


What is Electrostatic Discharge?

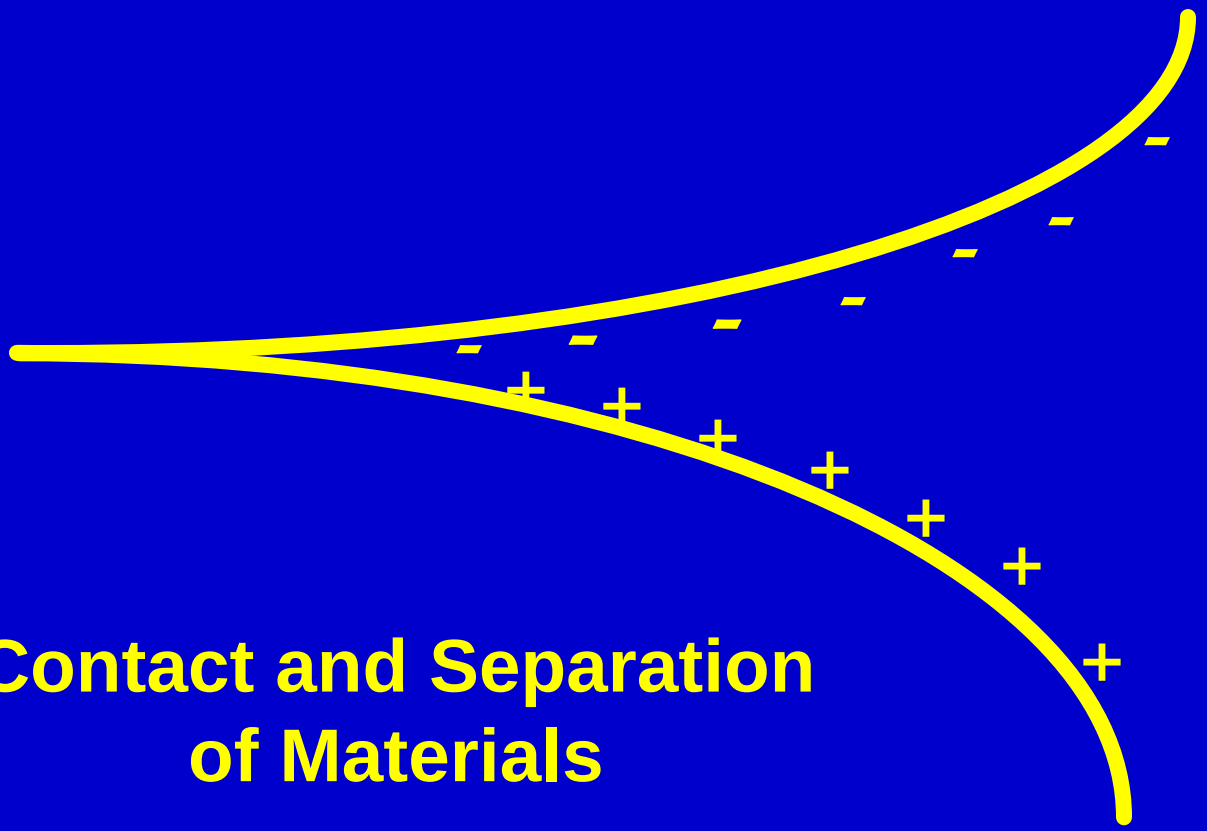
Purpose

- To understand what Electrostatic Discharge (ESD) is and what it means to electronics applications
- To define how the semiconductor industry takes precautions to minimize the threat to electronics
- To understand how silicon technologies are advancing and what the impact is on ESD and for future of the electronics

Outline

- What is Electrostatic Discharge (ESD)?
- ESD Control Methods
- Why is ESD important for semiconductor Integrated Circuit (IC) components?
- The impact of ESD on Electronic Systems
- Advances in silicon technology and the impact on ESD
- Advances in IC packages and the influence on ESD reliability
- Future research opportunities

How is Static Generated?



Contact and Separation of Materials

Electrostatic Charge Transfer

Triboelectric charging is the transfer of electrons between materials

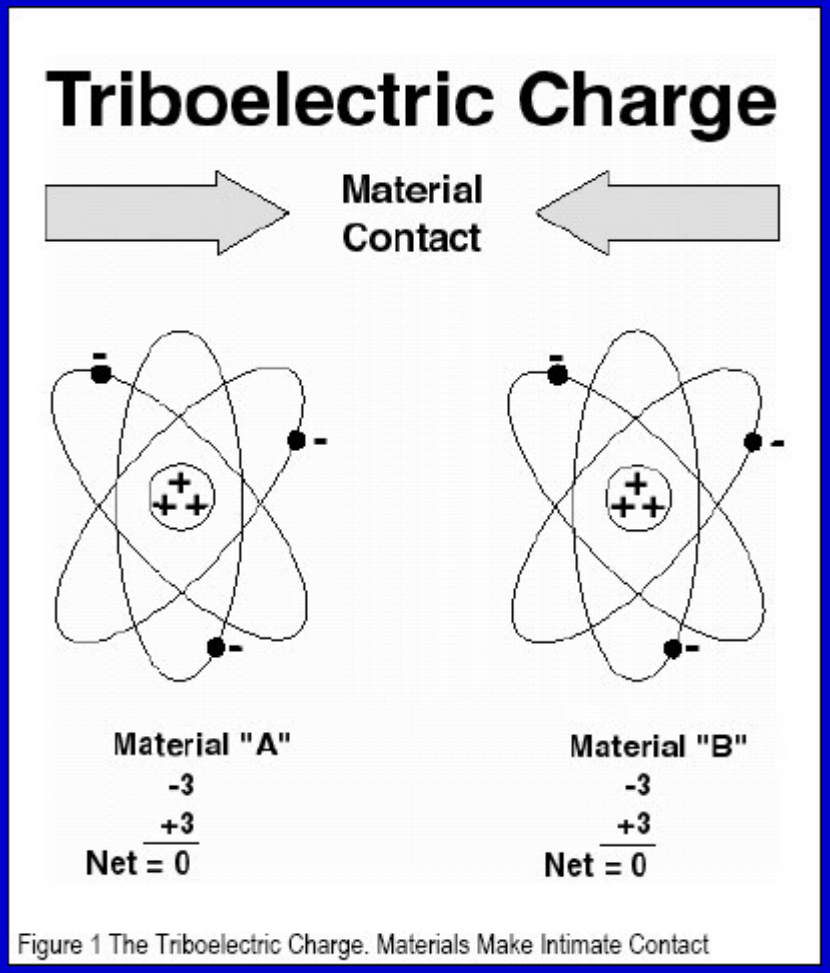


Figure 1 The Triboelectric Charge. Materials Make Intimate Contact

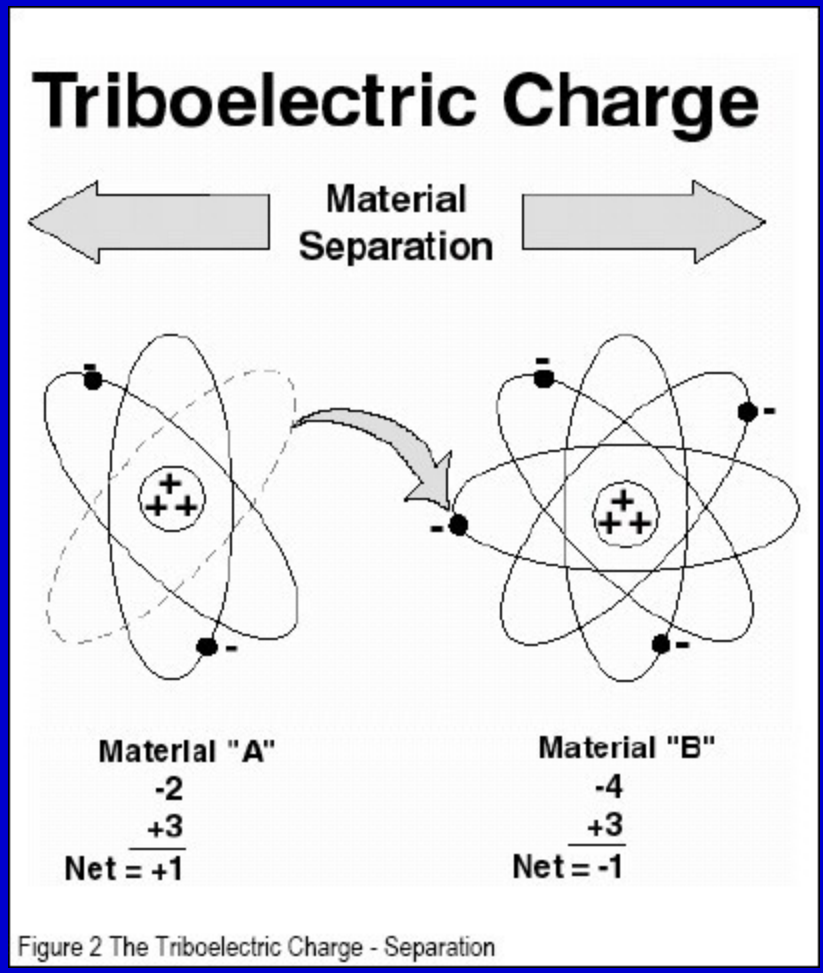


Figure 2 The Triboelectric Charge - Separation

The material that looses electrons becomes positively charged and the material that gains electrons becomes negatively charged.

Definitions

- **Electrical Overstress (EOS)**

  The exposure of an object to a current or voltage beyond its maximum ratings.

- **Electrostatic Discharge (ESD)**

  The transfer of electrostatic charge between bodies or surfaces at different electrostatic potential. ESD is a subset of EOS.

ELECTROSTATIC DISCHARGE (ESD)

What is Electrostatic Discharge?

- The sudden discharge of a charged body
- Tribo-electric and induced charging

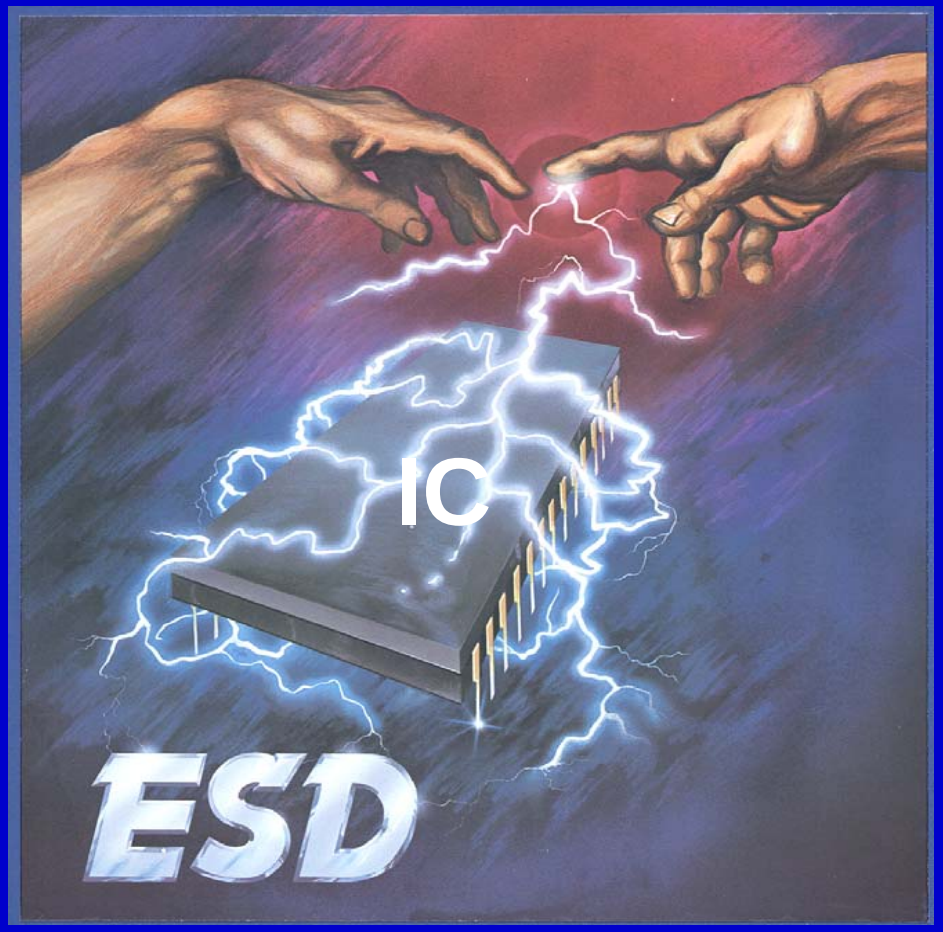
Importance of ESD to the Semiconductor Industry

- Unexpected destruction of semiconductor devices
- Losses can occur anywhere from fabrication to field
- Millions of dollars in real losses each year
- Unknown amount of hidden losses each year

A BRIEF REVIEW OF THE HISTORY OF ESD

- On this planet, static electricity has been a curiosity for magicians to pseudo-scientists for many hundreds of years.
- Static sparks needed special precautions in manufacturing of gun powder.
- Static electricity became a problem for the film industry in the 40's and 50's and for the electronic industry in the 50's and 60's. It became worse with newer technologies in the 70's, it is becoming even more critical ever since…
- Today many industries or organizations take special care for ESD or for static sparks.

Dinosaurs to ICs can suffer from ESD



Definitions

EOS General

High Voltage (1V –15kV)
Short Duration
Very Low Power
Fast Rise Time
(1-10 ns)

Low Voltage (16V)
Longer Duration
Low Power
(1-10 ms)

Extremely High Voltage
Extremely High Power

Integrated Circuit (IC) chips used in consumer and medical electronics can be damaged with ESD

Houses, Buildings Airplanes, Electronics, etc.

What voltage levels are generated if ESD is not controlled?

CONDITION	AVERAGE READING(V)
Person Walking Across Linoleum Floor	5,000
Person Walking Across Carpet	15,000
Person Working at Bench	800
Ceramic Dips in Plain Plastic Tube	700
Ceramic Dips in Plastic Set-Up Trays	4,000
Ceramic Dips in Styrofoam	5,000
Circuit Packs as Bubble Plastic Cover Removed	20,000
Circuit Packs as Packed in Foam Box	11,000
Circuit Packs (Packaged) as Returned For Repair	6,000

UNGER, 1981 IRPS

But, humidity helps reduce static charge generation and accumulation

(values shown in volts)

Event	Relative Humidity		
	10%	40%	50%
Walking across a vinyl floor	12,000	5,000	3,000
Motion of bench employee	6,000	800	400
Removing ICs from plastic tube	2,000	700	400
Packing PWBs in foam line box	21,000	11,000	5,500

* TED DANGELMAYER, *ESD PROGRAM MANAGEMENT*, KLUWER ACADEMIC PUBLISHERS, 1999

It can be controlled by materials

Bad

- **INSULATIVE: Non-conductive, removed from workplace whenever possible. (> 1x10e12 Ohms)**

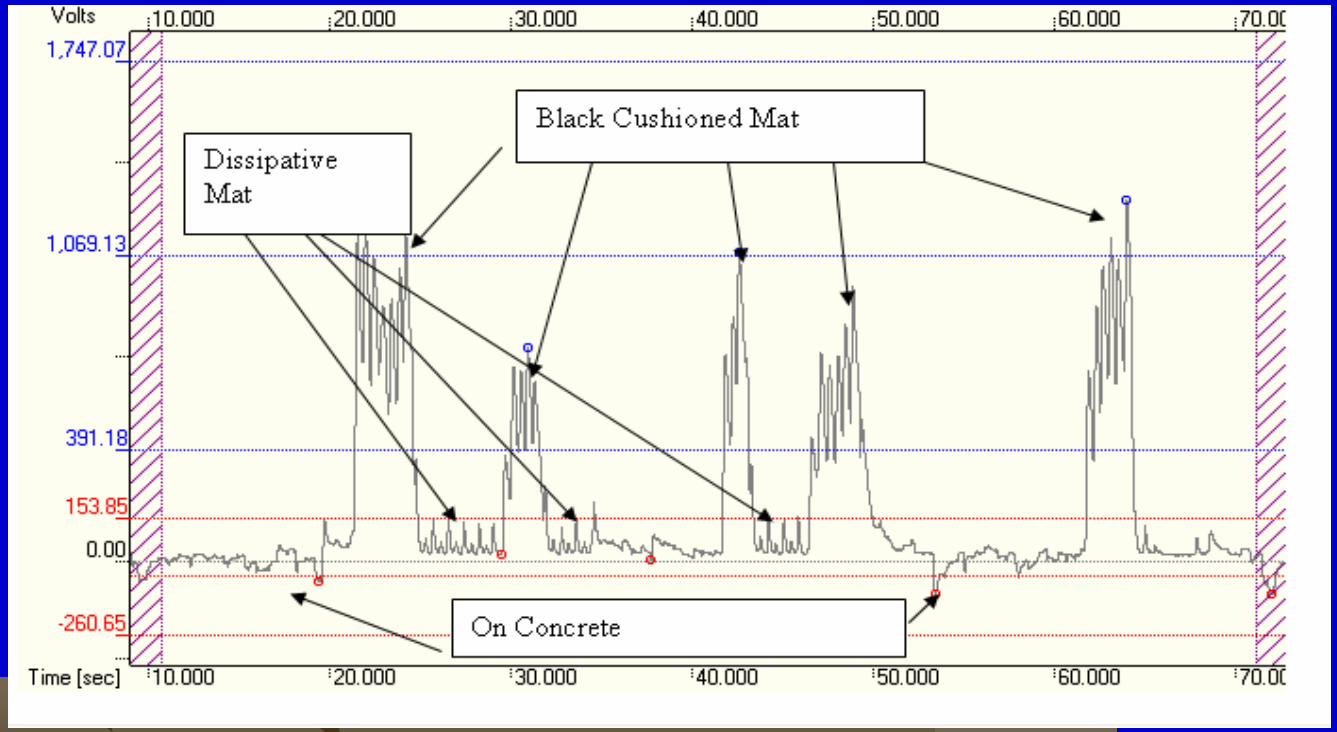
Not so bad

- **CONDUCTIVE: Lowest surface resistance. (<10e4 Ohms)**

Good

- **DISSIPATIVE: Bleeds off charges at optimum rate. Strongly preferred. (10e4 to < 10e11 Ohms)**

If it is not properly controlled in a silicon manufacturing environment…



Thousands of volts can be generated

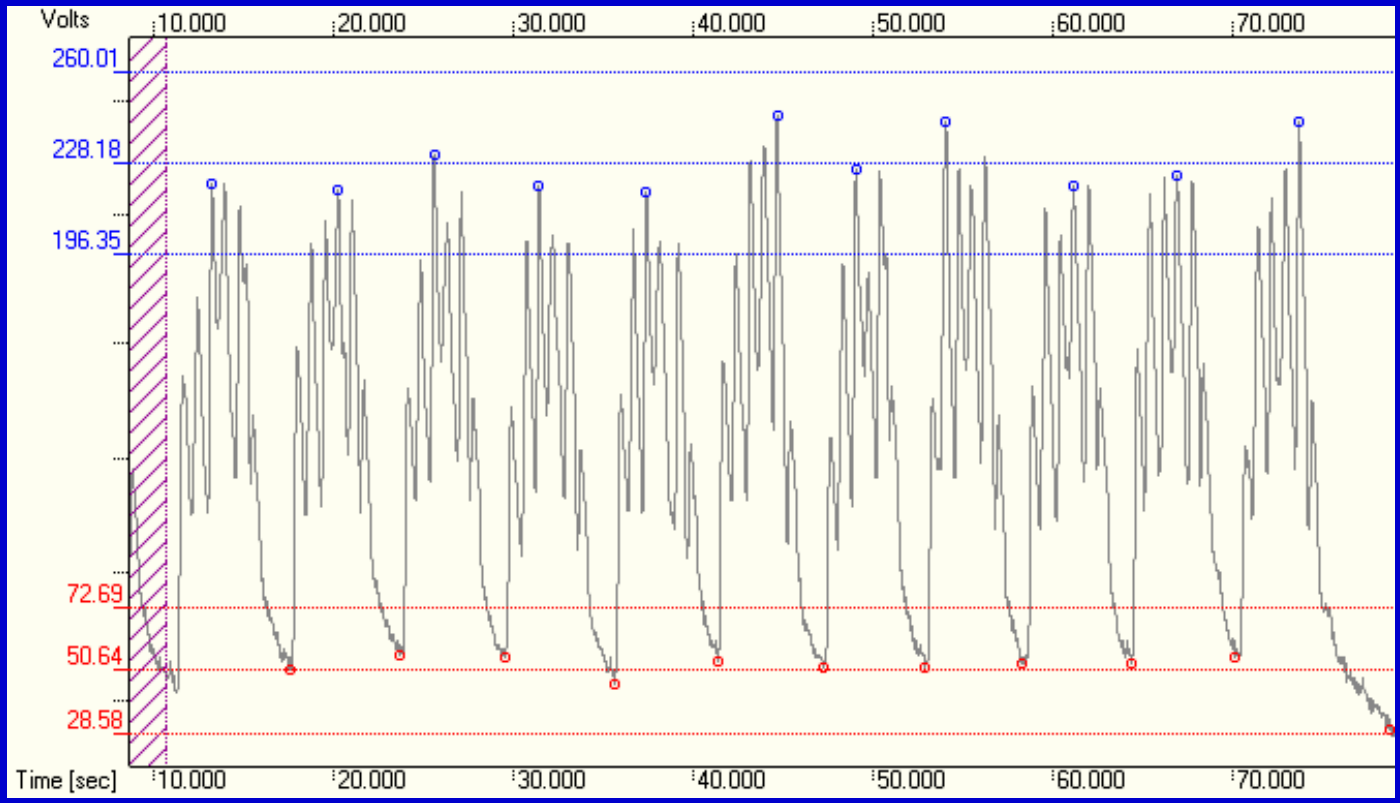
How is ESD controlled?

1 Grounding Person
Wrist Strap to Ground
(or flooring/footwear)

2 Grounded Work Surface

3 ESD Protective
Packaging

With good ESD control the levels are lower

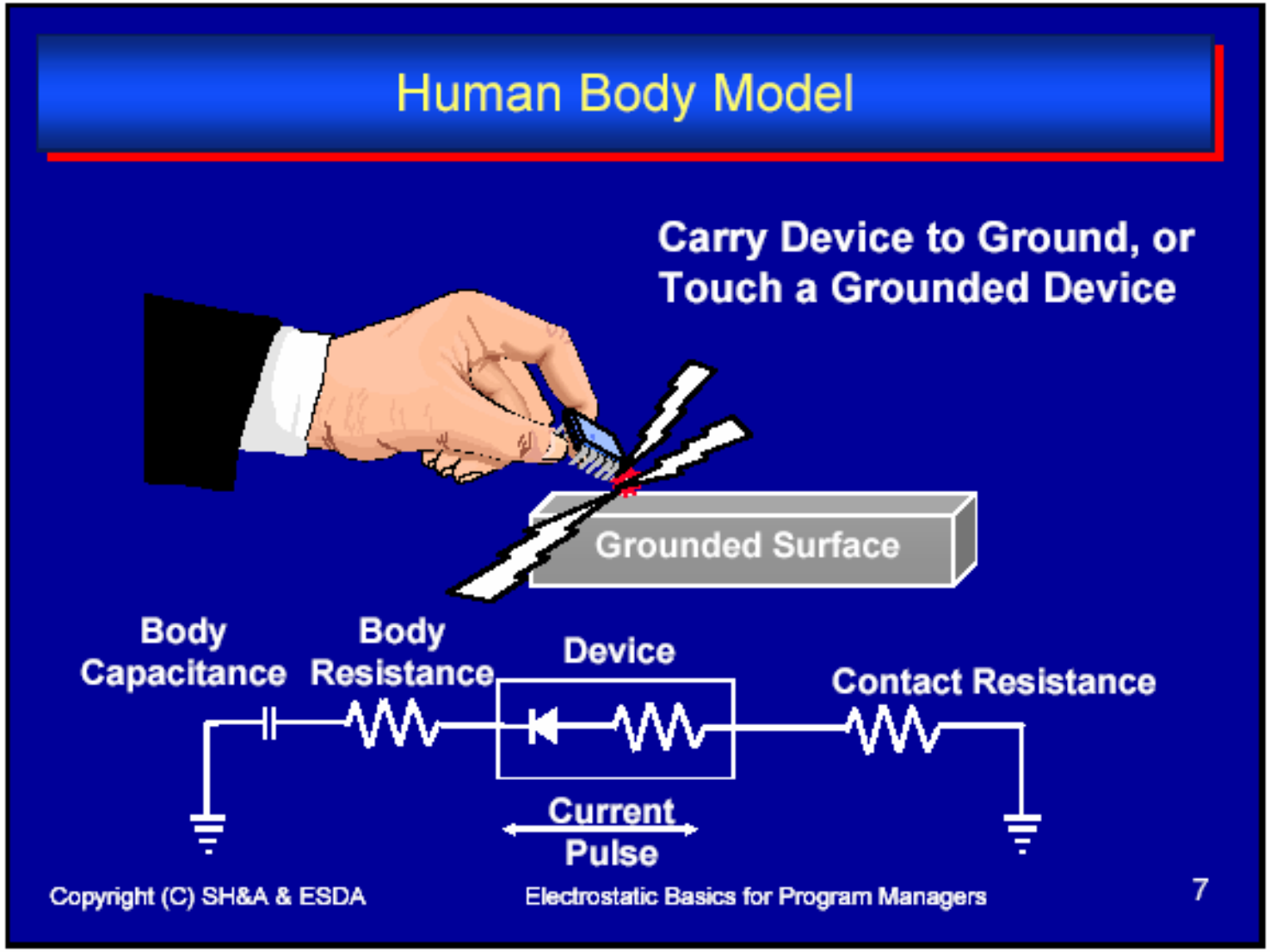


Only hundreds of volts are generated

IC Package Impact on ESD

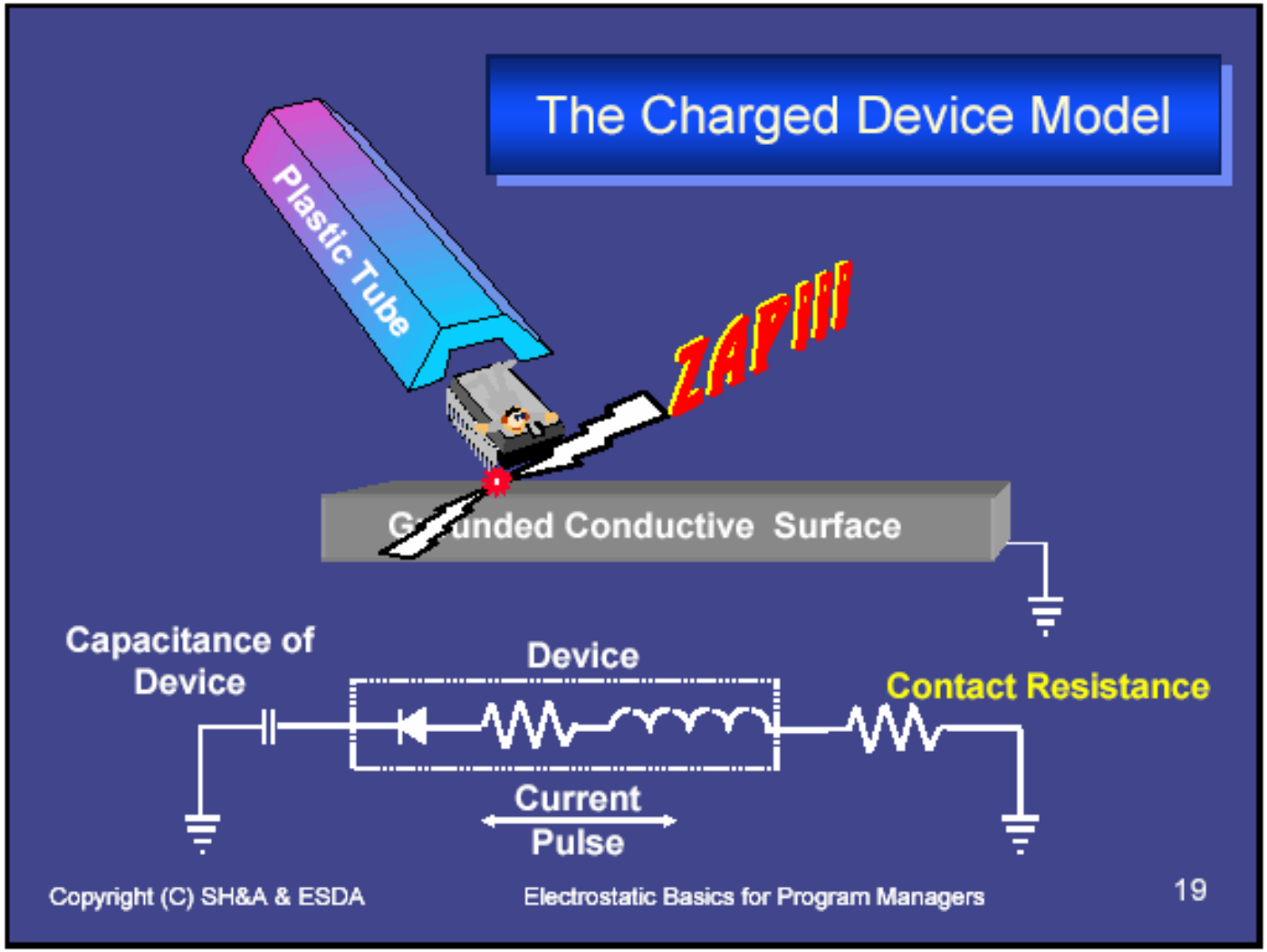
- IC packages can have impact on ESD requirements for
  - Human Body Model (HBM)
    - Exposed IC package pins can be touched during normal handling
  - Charged Device Model (CDM)
    - IC packages that acquire charge in automated handlers can discharge with contact to ground

Human Body Model



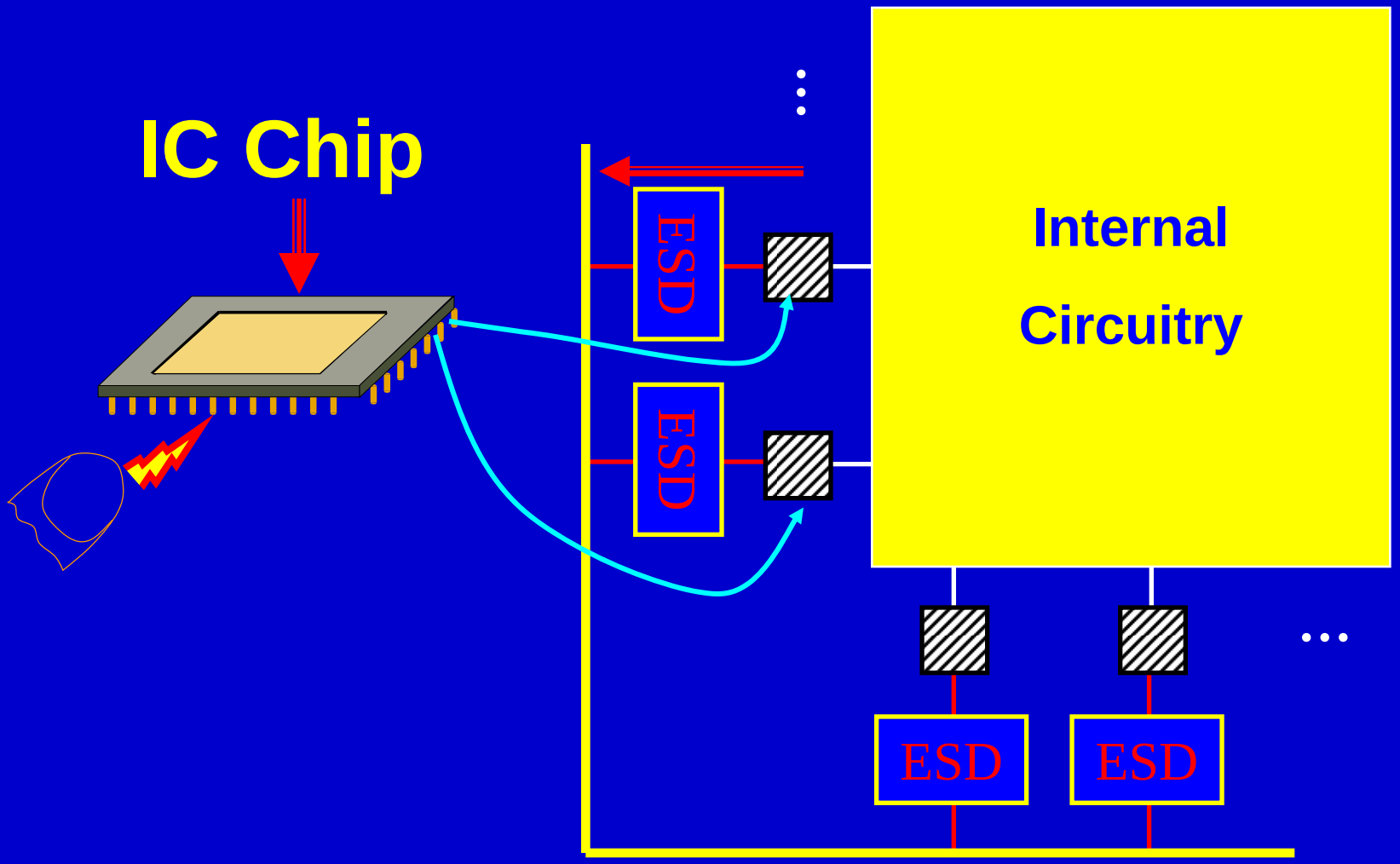
C. Duvvury

Courtesy: ESD Association

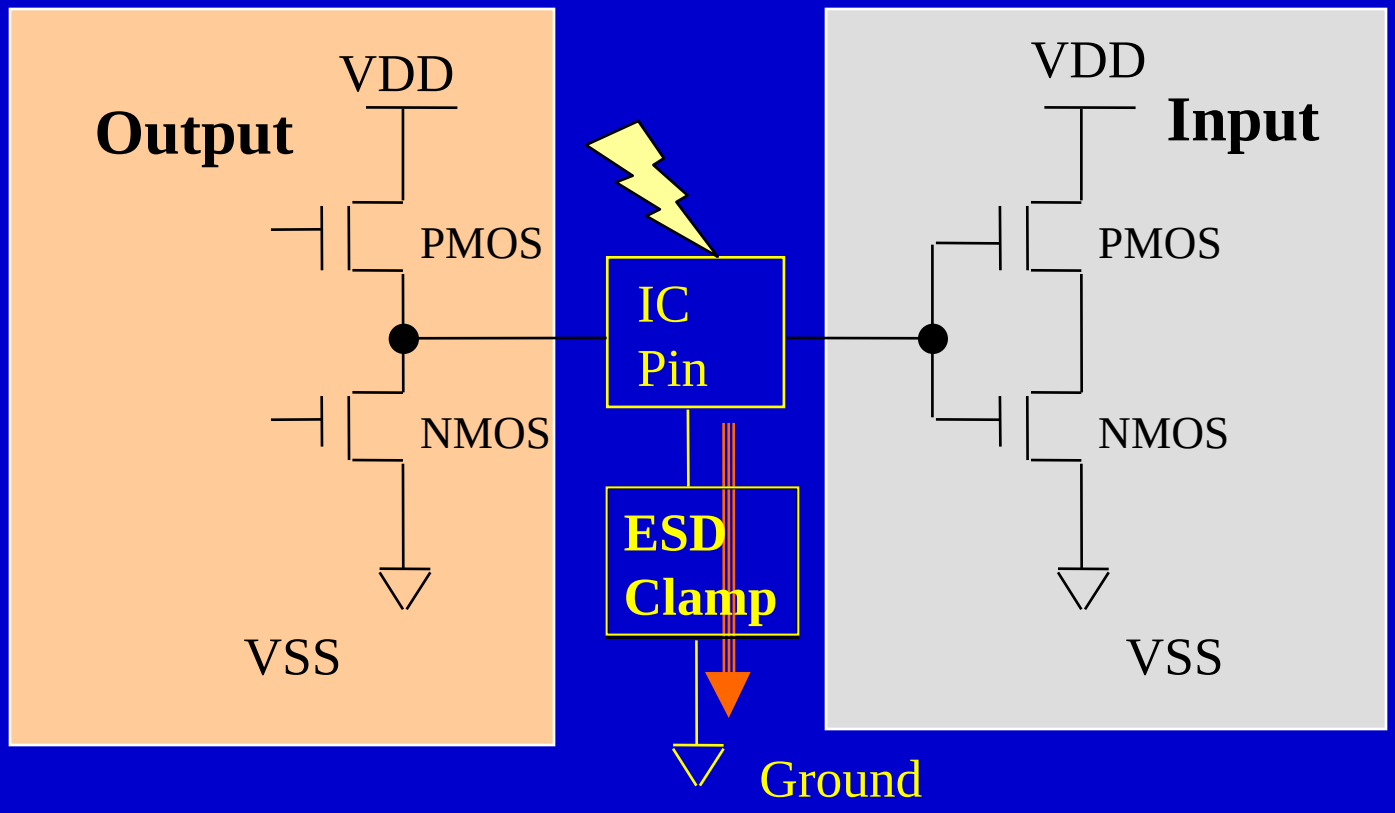


Courtesy: ESD Association

IC Chip pins are protected with protection devices (diodes) on the chip



On-Chip Protection Design

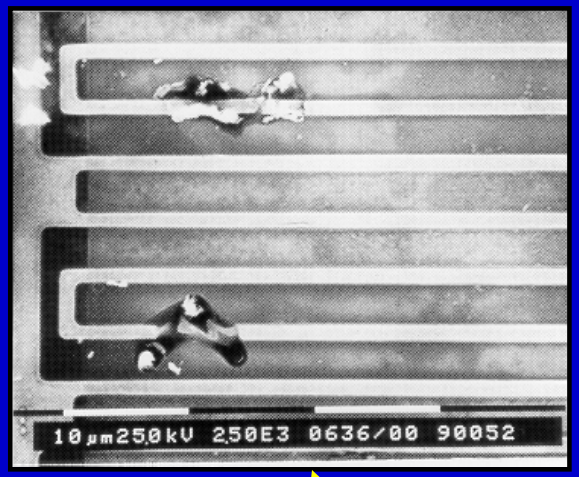


The Input and Output pins of the IC protected from ESD

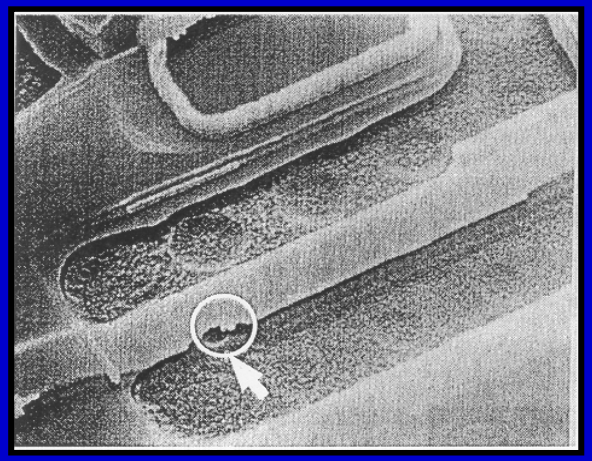
The clamp turns only when ESD is detected

These clamps introduce capacitance and reduce circuit speed

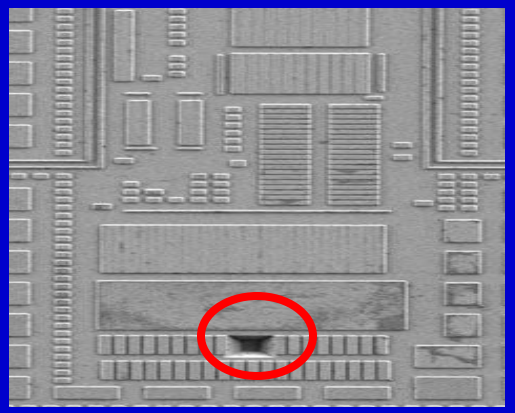
What if the IC pins are not adequately protected?



Damage to transistors



Damage to insulating oxides



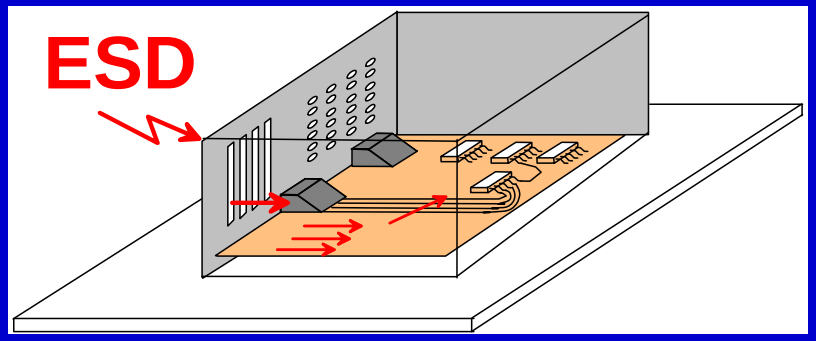
Damage to internal circuits

With IC pin damage the chips would not function in a system

What about touching the systems themselves?

Electric and magnetic fields produced by ESD couple to the system in multiple ways, causing failures.

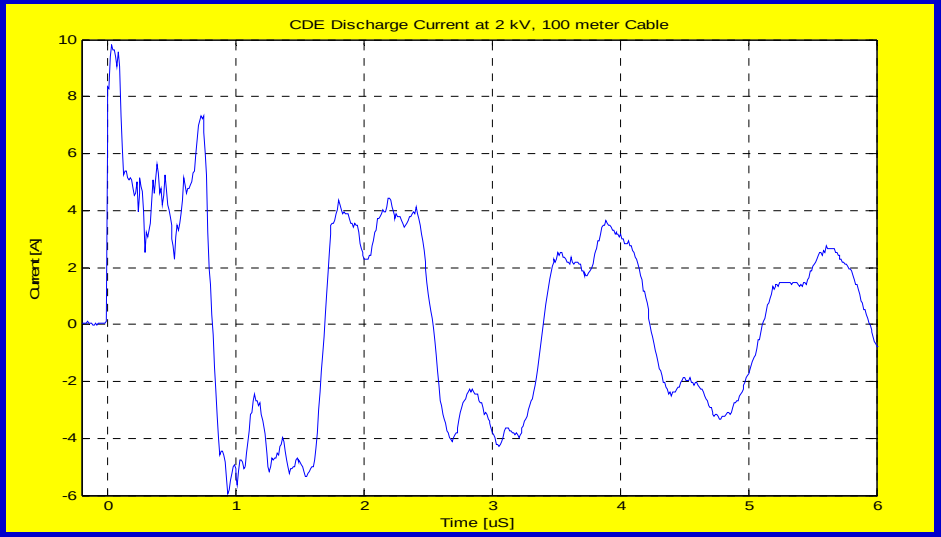
A human holding a metallic object (e.g. keys, screwdriver) discharging accumulated static charge through an electronic product (e.g. cellular phone, computer).



Cable Discharge During Computer Connections

- Cables could acquire electrostatic charges primarily due to tribo-charging
- A discharge could occur when a charged cable is plugged into an electronic equipment
- The electronics inside must be protected

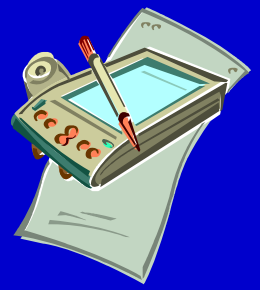
Discharge from a 100m long cable charged to 2000V



ESD on Systems

Any electronic equipment can be damaged by ESD

"End Equipment"



PDAs

Cell Phones

Corded Phones

Computers

Printers

Copy machines

Automotive electronics

Telephone Switching gear

… any electronic end product!

Digital Electronics…

Increasingly becoming part of daily lives

Music, Movies, TV Shows, Home Video, Photos, Audiobooks, Podcasts


…At Home

Consumers just want to turn it on and enjoy high quality digital content

Real Time A/V streaming, Data/Control, Decoder/Encoder, Content Protection

…On the Road

We need to make sure all electronics are protected!

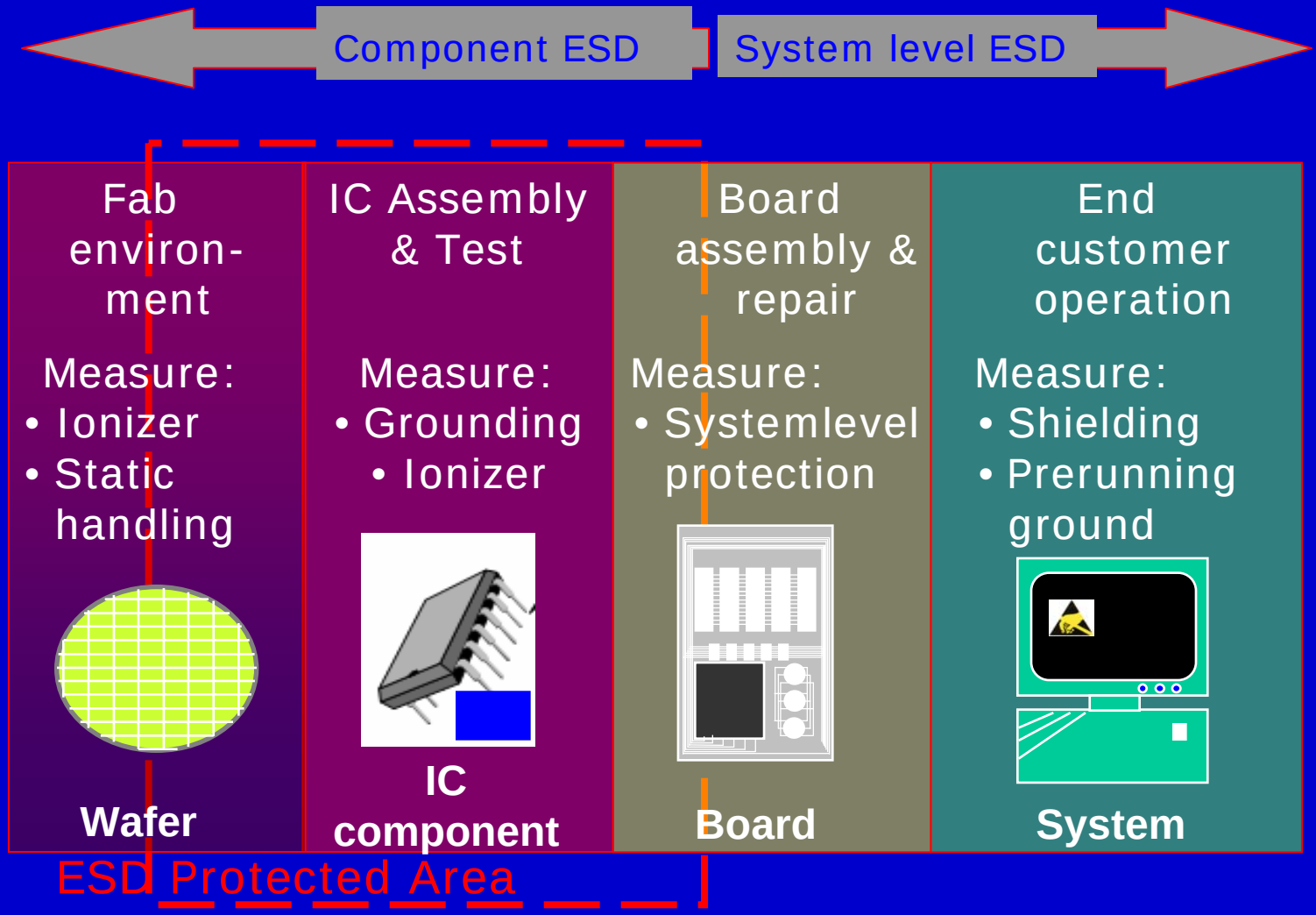








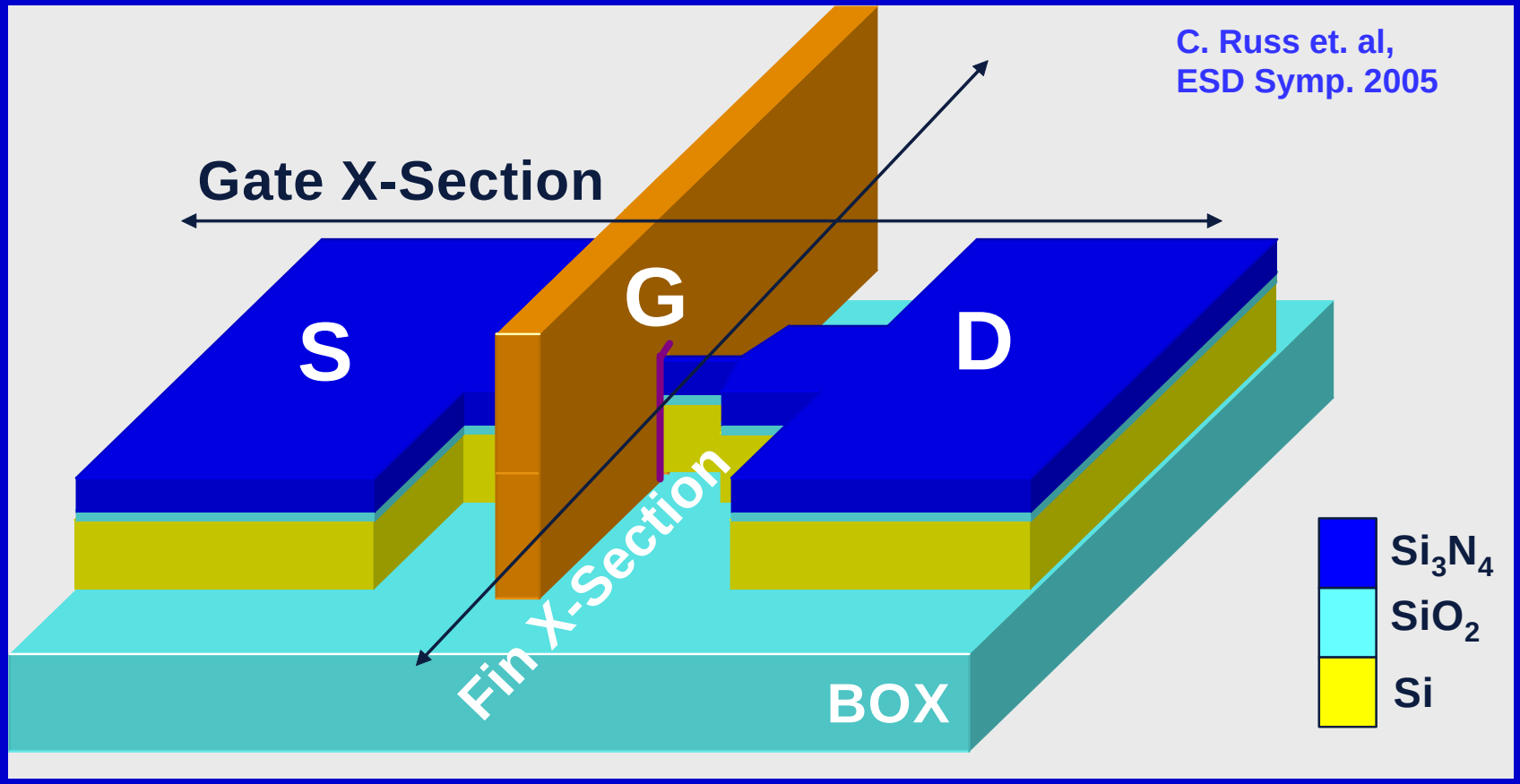

Stages of ESD Protection Methods and Design



Silicon Technology Advances and Challenges…

- Smaller transistors (<100 nm feature sizes) for higher speed circuits (5-10 GHz)
  - These transistors are much more delicate for ESD protection
- Complex circuit designs with multiple functions on the same chip
  - Continuous challenge to protect them and still maintain high speed performance
- Larger and advanced IC packages producing higher current levels during discharge
  - Making sure all types of packages are equally protected

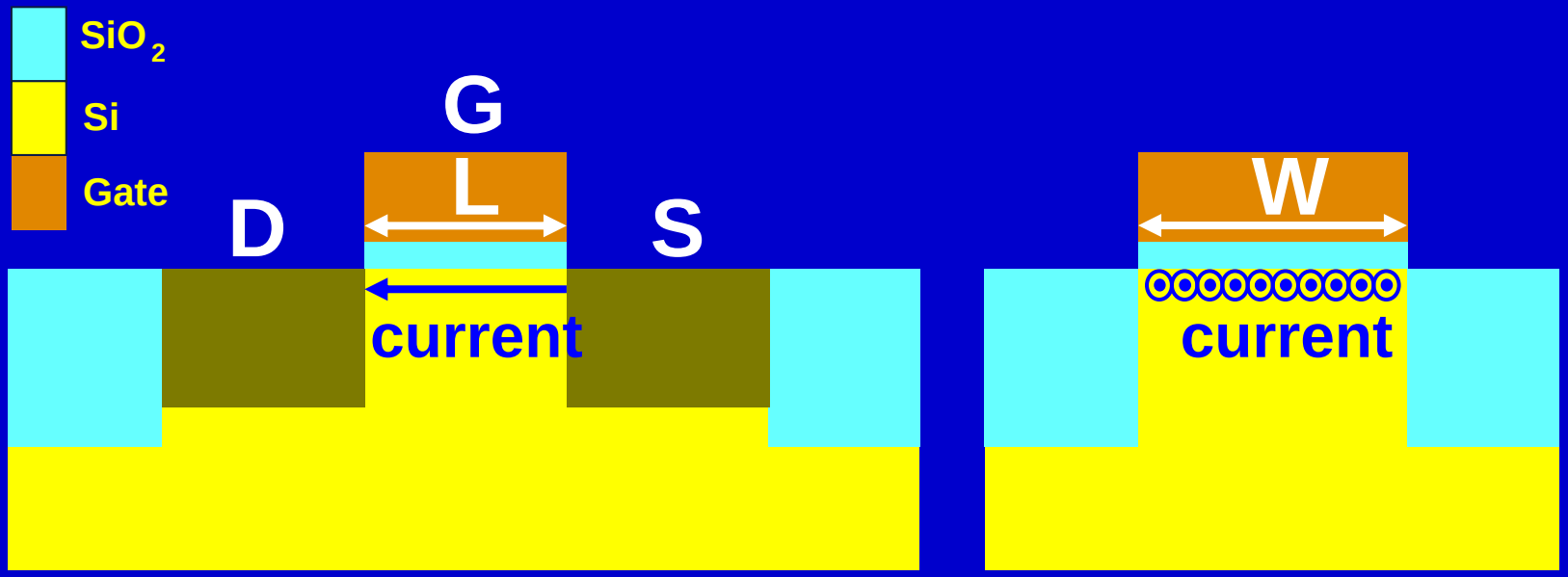
3-D Transistors of the Future



These transistors are built on top of silicon-on-insulator

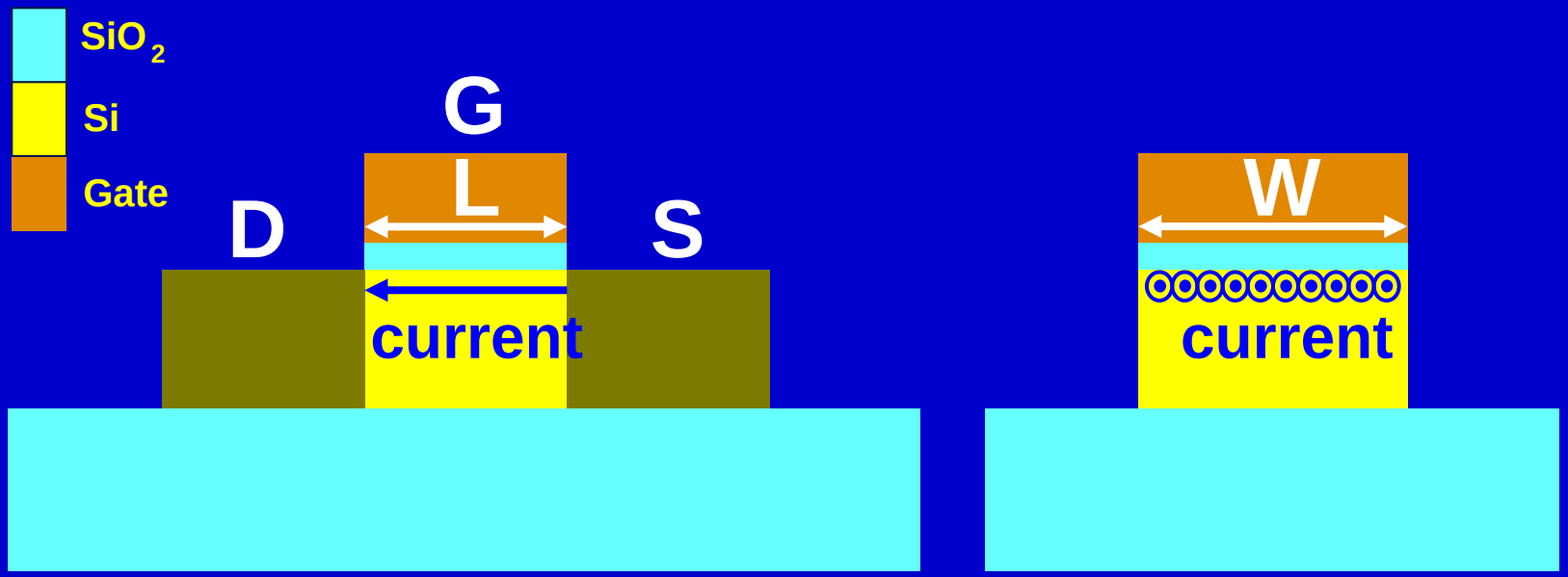
These devices are expected to be very sensitive to ESD

Classical FET in Bulk Si



- **Scaling expected to become difficult due to Short Channel Effects (32nm node and beyond)** **C. Russ ESD Symp. 2005**

Planar FET Device in SOI



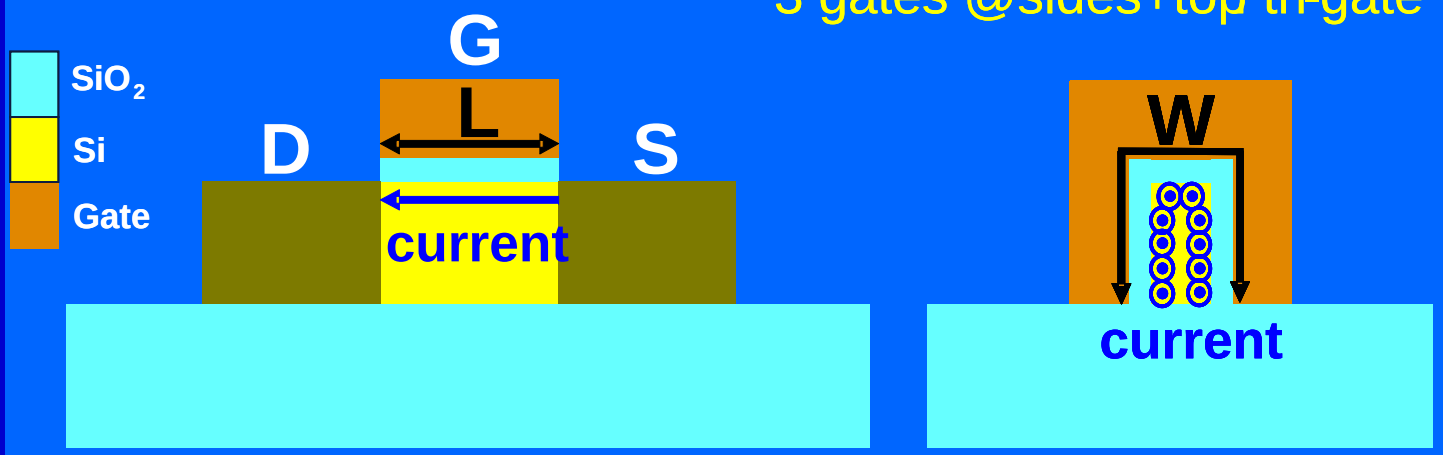
- Low junction capacitance → speed!
- Good body control in fully depleted SOI

C. Russ ESD Symp. 2005

MuGFET Device (or "FIN"-FET)

2 gates @ sides: double-gate

3 gates @sides+top tri-gate



- Channel enclosed by multiple (2, 3, 4) gates
  → Best body control (fully depleted)
  → Suppression of Short Channel Effect
- Best candidate for continued technology scaling

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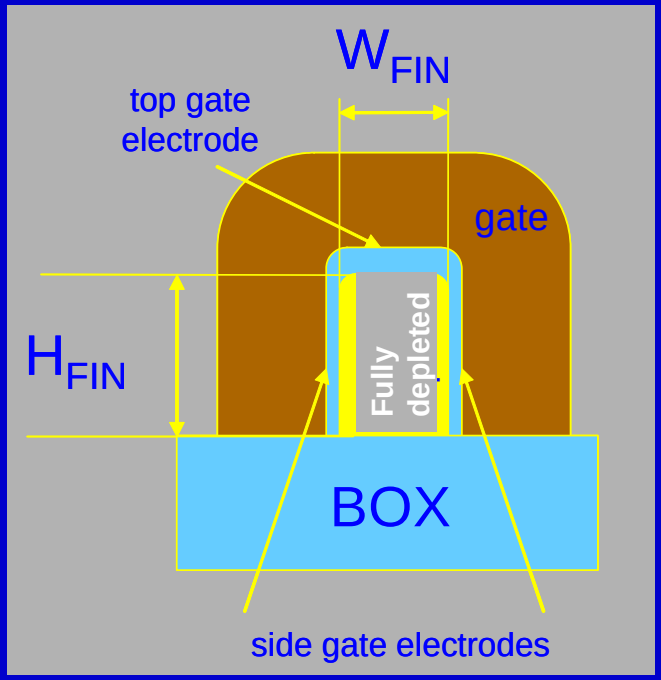
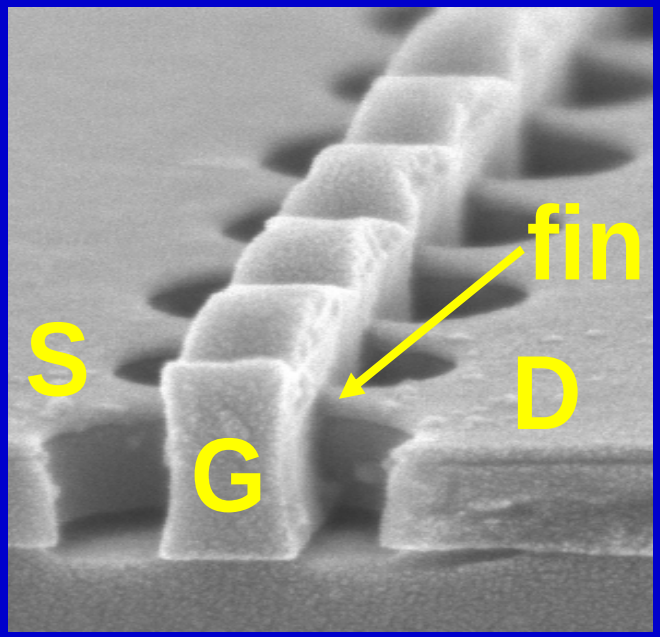
Multi-gate Transistors (MUGFETs) with very small dimensions

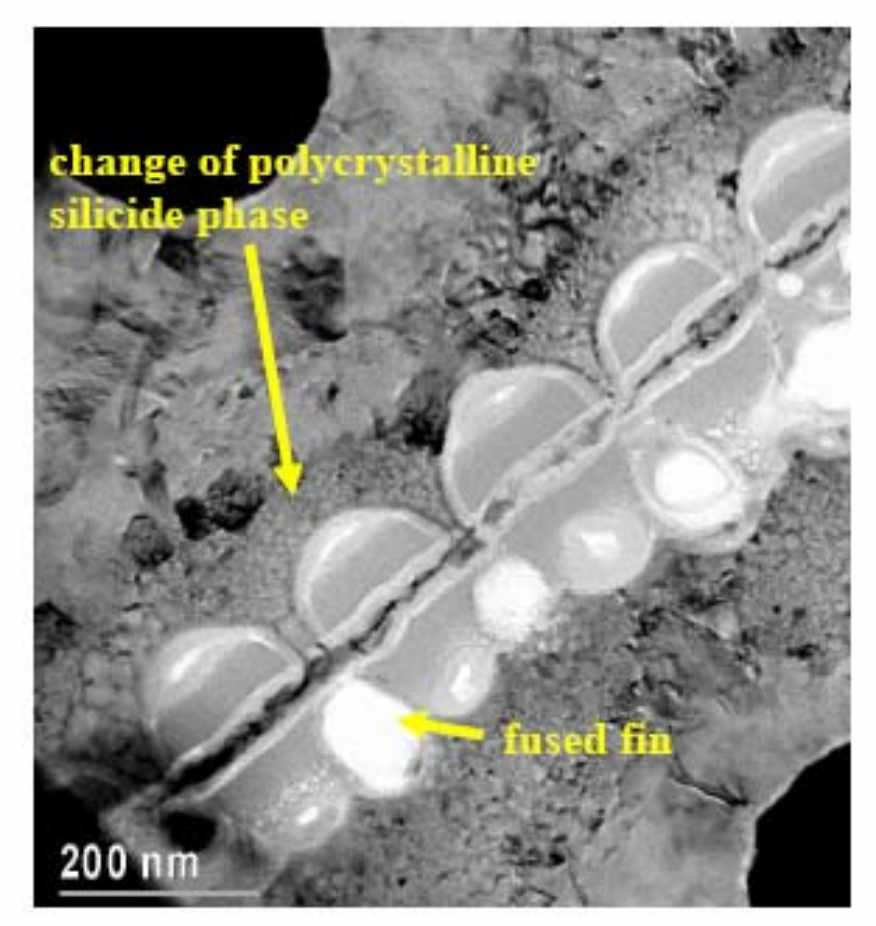




- **Fin height: 66-80nm (present), 30-40nm (target)**
- **Fin width: 50nm (present), 20-30nm (target)**
- **Capability to carry ESD current?**

C. Duvvury **C. Russ ESD Symp. 2005**

MuGFET: Damage Under ESD



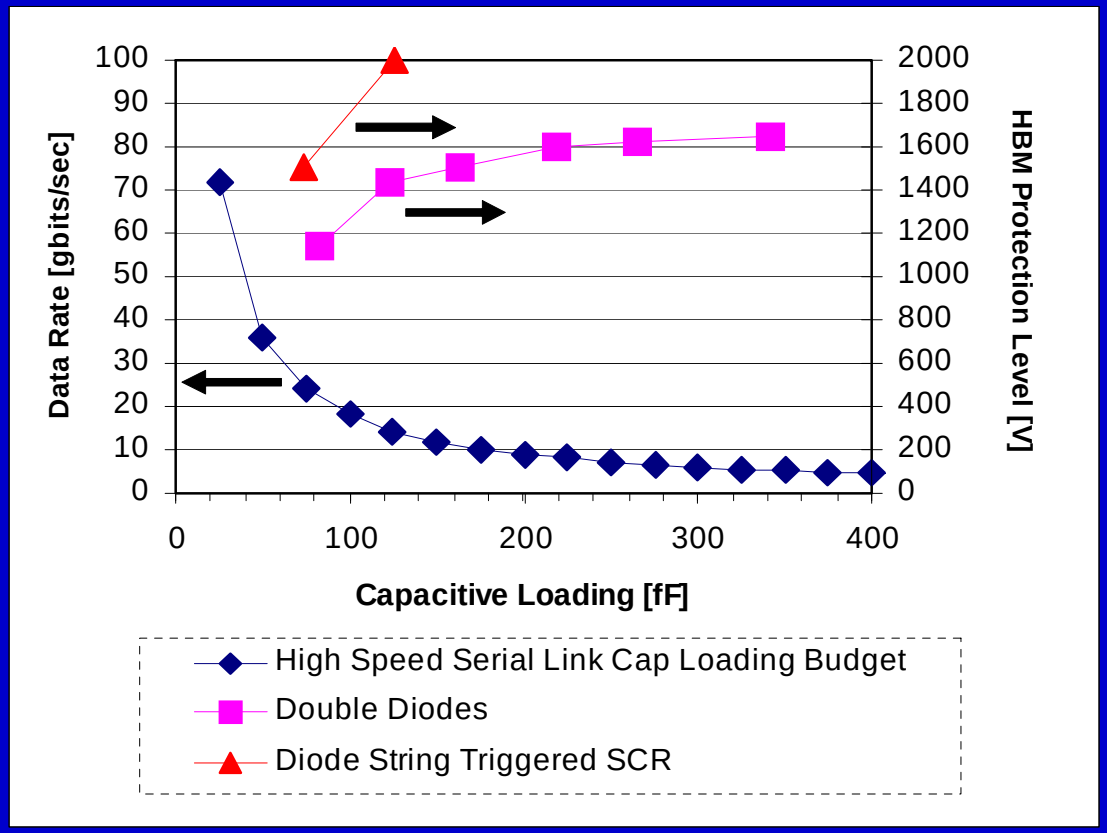
- Unprecedented high ESD sensitivity
- Fused fins if process is not optimized

H. Gossner IEDM 2006

Circuit Challenges: New Designs

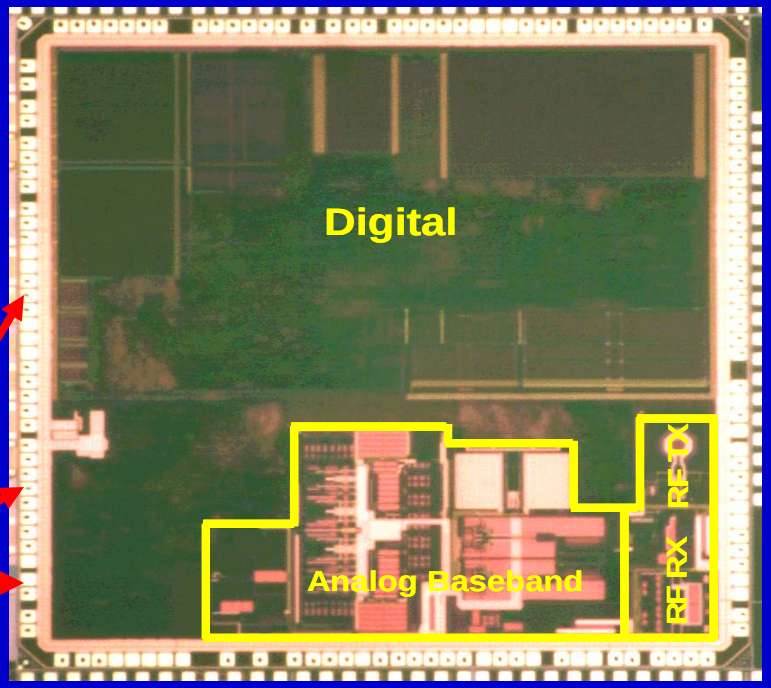
- Increased Analog IO applications
- Analog Integration
- High speed IO interfaces
- Increased RF integration
- New IO features
- USB applications

Example: Impact of ESD protection on circuit speed



- **Data Rates are influenced by the loading capacitance**
- **The capacitance in turn degrades ESD levels**

System on a Chip



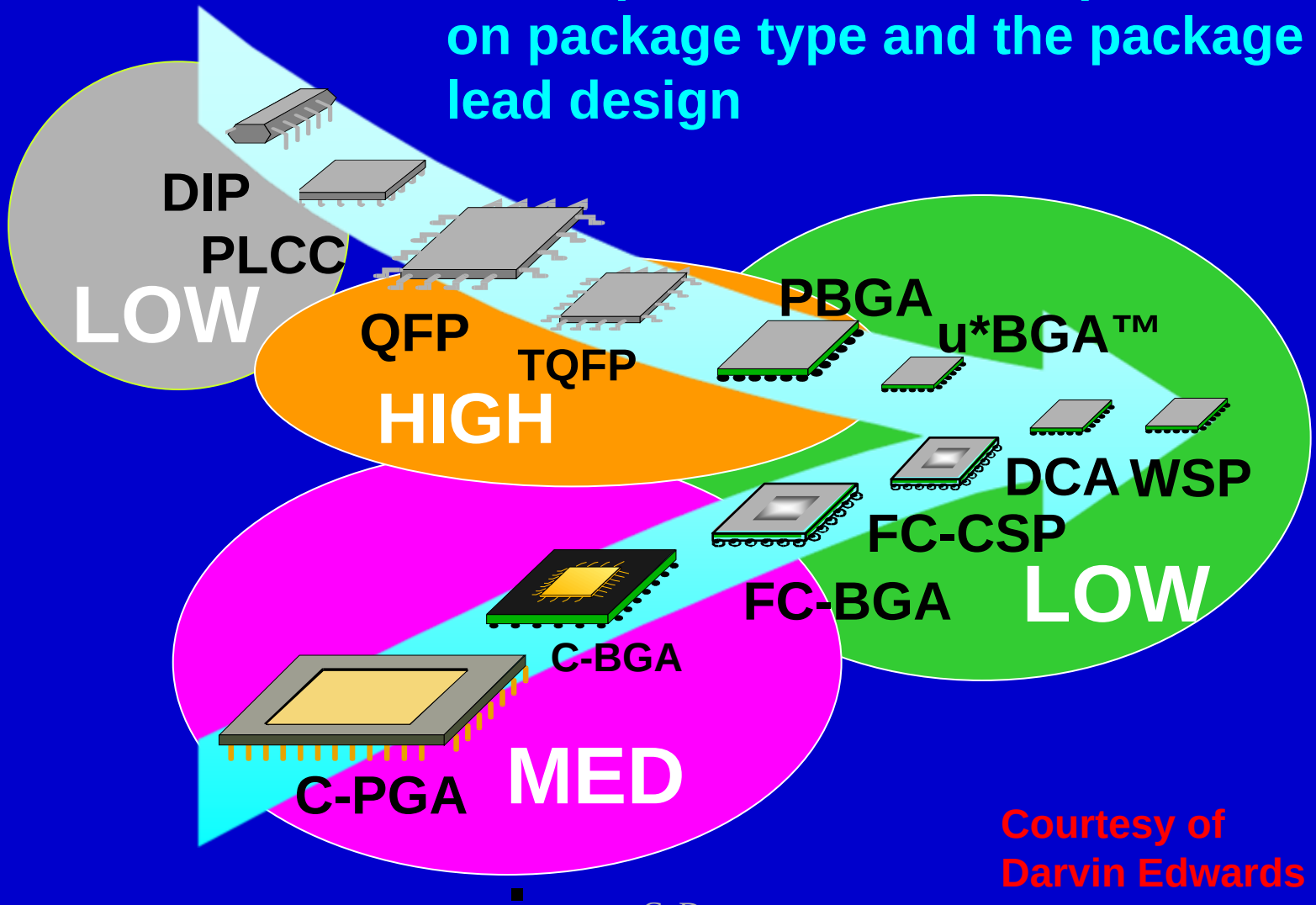
Every pin needs protection

Bluetooth Chip

- Digital, Analog, and RF on the same chip require three different ESD protection strategies
- Interactions through the different ground planes require complex ESD bus architecture

ESD Risk Versus Package Type

- ESD performance is dependent on package type and the package lead design



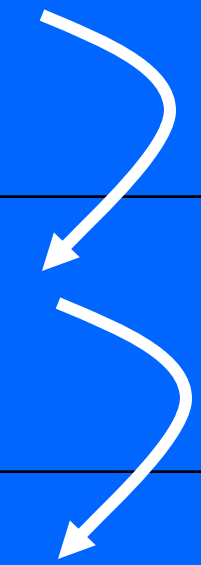
Courtesy of Darvin Edwards (TI)

Technology Scaling Effects: IC Packages

Technology Node	Common Packages	New Developments	Comments on ESD
3-5 um	DIP TQFP QFP	-	DIP devices relatively more sensitive to HBM
1 um	DIP TQFP QFP	PBGA Flip-Chip-BGA	TQFP more sensitive to CDM than the BGA's
1 um to 100nm	TQFP QFP	2000 pin Flip-Chip Packages	Large pin count devices very harsh for CDM protection

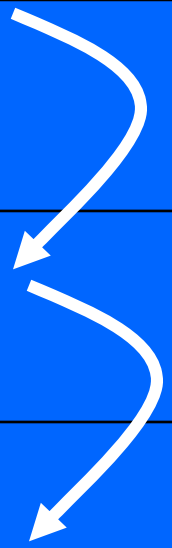
IC Package Impact on ESD

Technology Node	Common Packages	New Developments	Comments on ESD
3-5 um	DIP TQFP QFP	-	DIP devices relatively more sensitive to HBM
1-2 um	DIP TQFP QFP	PBGA Flip-Chip-BGA	TQFP more sensitive to CDM than the BGA's
1 um - 0.5 um	TQFP QFP	2000 pin Flip-Chip Packages	Large pin count devices very harsh for CDM protection



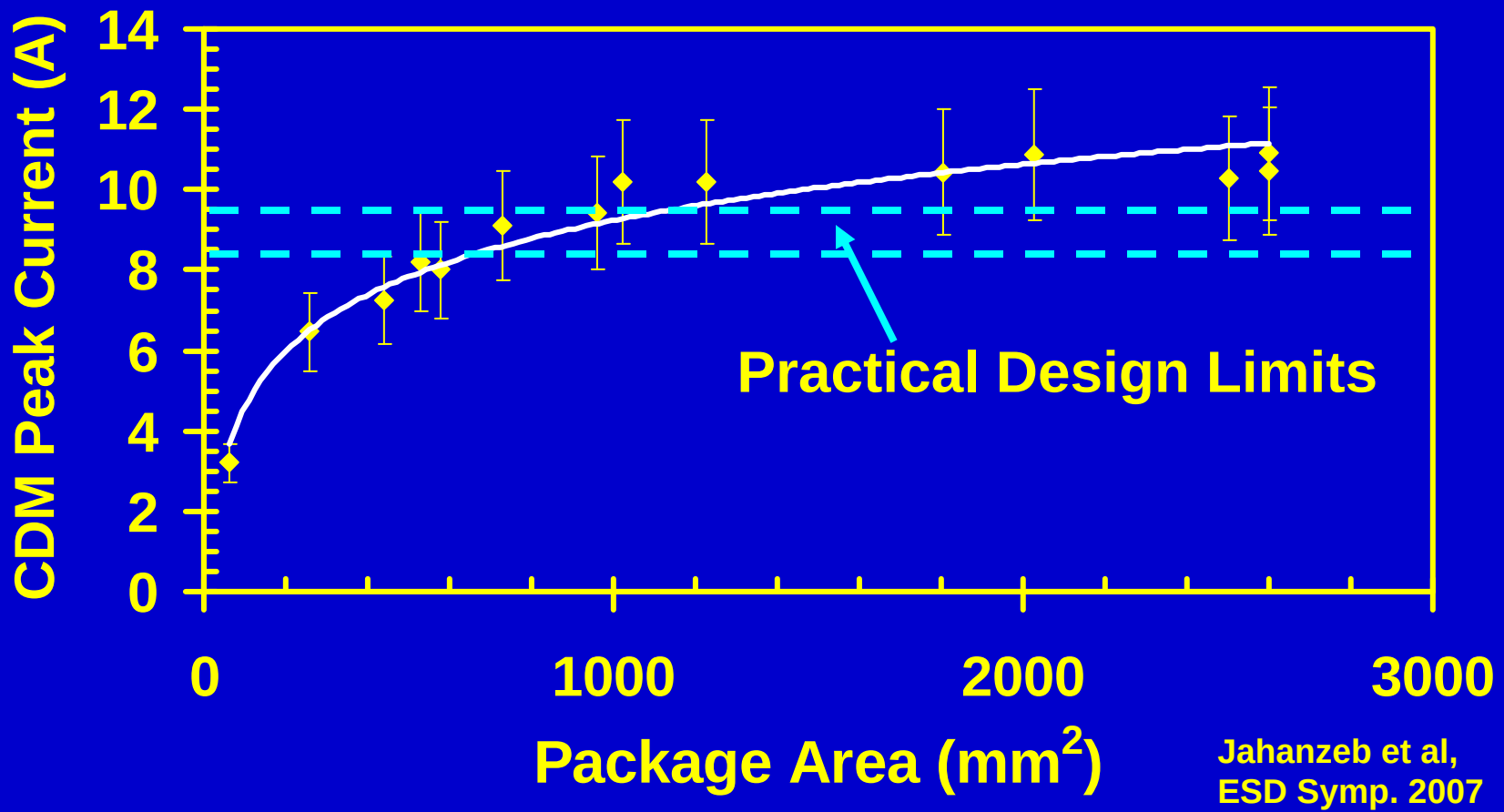
IC Package Impact on ESD

Technology Node	Common Packages	New Developments	Comments on ESD
0.5 um	TQFP QFP BGA	Stacked Die / Stacked Packages	Complexity in ESD testing
100 nm	BGA	Silicon Vias	Major challenge for ESD evaluation
<50 nm	No packages	Bare die	Unknown ESD evaluation



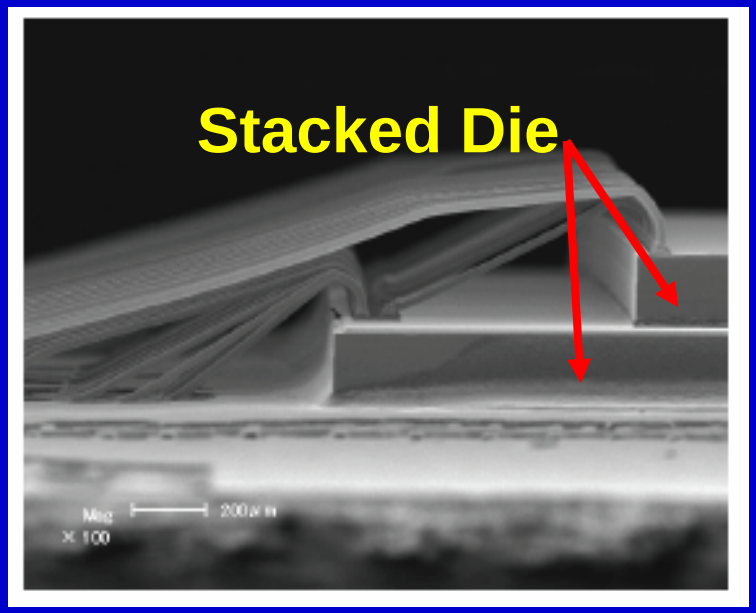
Package Size on ESD Current

CDM Peak Current at 500 V



Protection design is difficult for large packages!

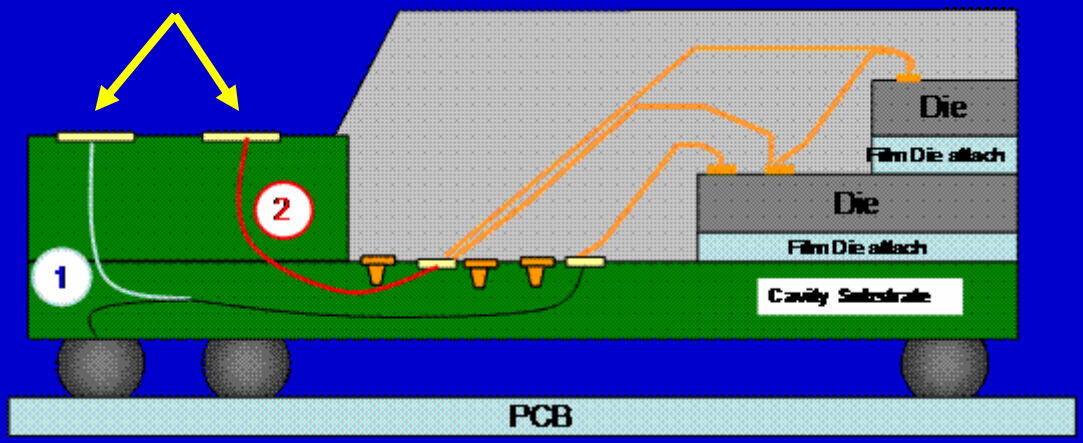
Stacked Die/Package Development



Both Stacked Die and Stacked Package trends can lead to unknown ESD stress discharge currents

Package on Package (POP)

Top Pads



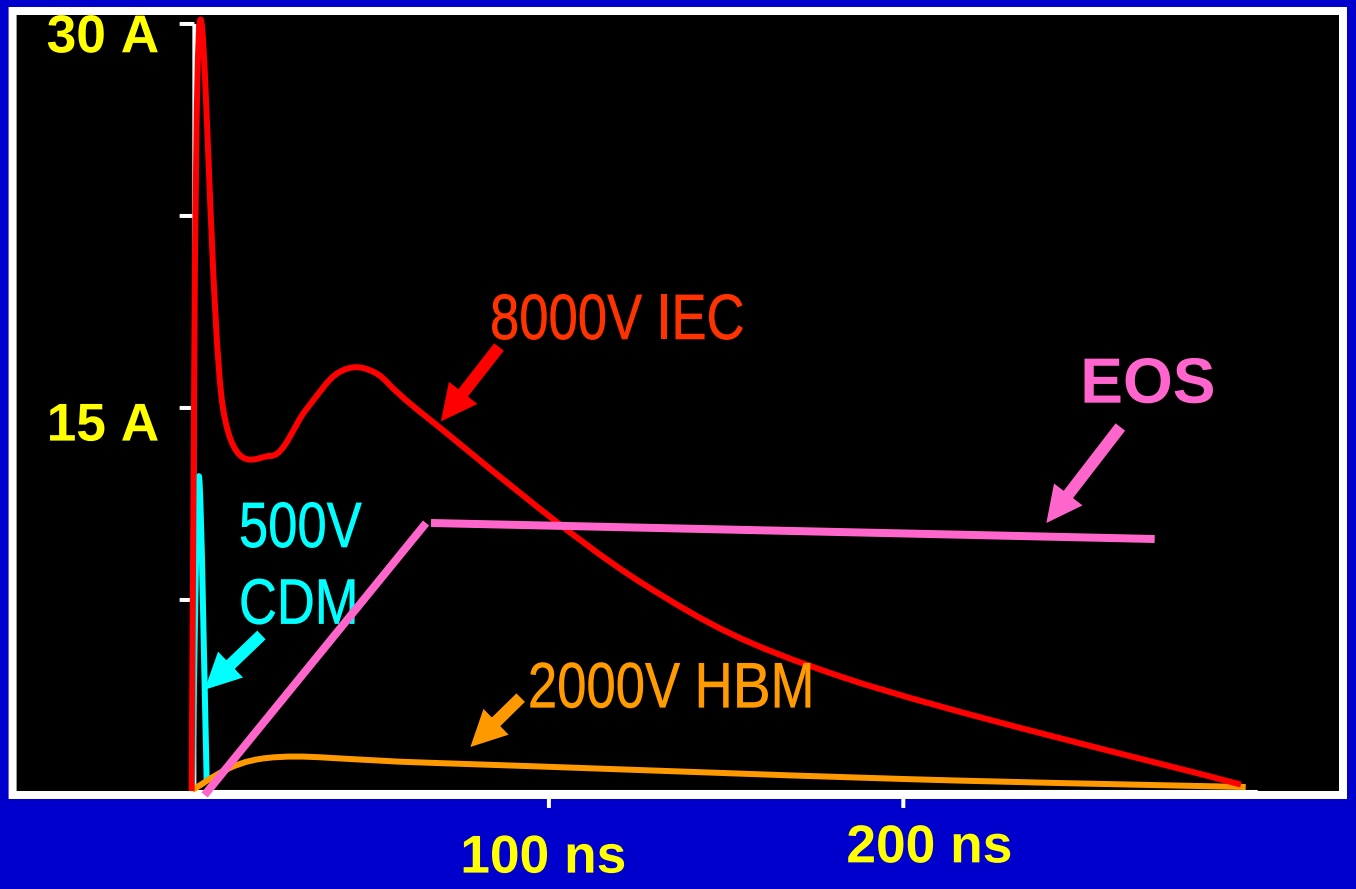
Complications with stacked die and stacked packages

Package ESD Sensitivity*

Condition	Classification	Sensitivity Scale
No IC Chip	Discretes	0 (None)
IC in Package	Memory OMAP Analog Digital	3 (Low)
IC in Package	CMOS BiCMOS	4 (Low)
IC in Package	65nm and beyond	6 (Moderate)
IC in Package	RF CMOS	7 (Moderate)
IC in Package	RF GaAs	8 (High)
IC in Package	5-10 GHz	9 (Very High)
Wafer Scale	TBD	9 (Very High)

ESD levels <500V HBM are considered sensitive

Transient Stress Modes

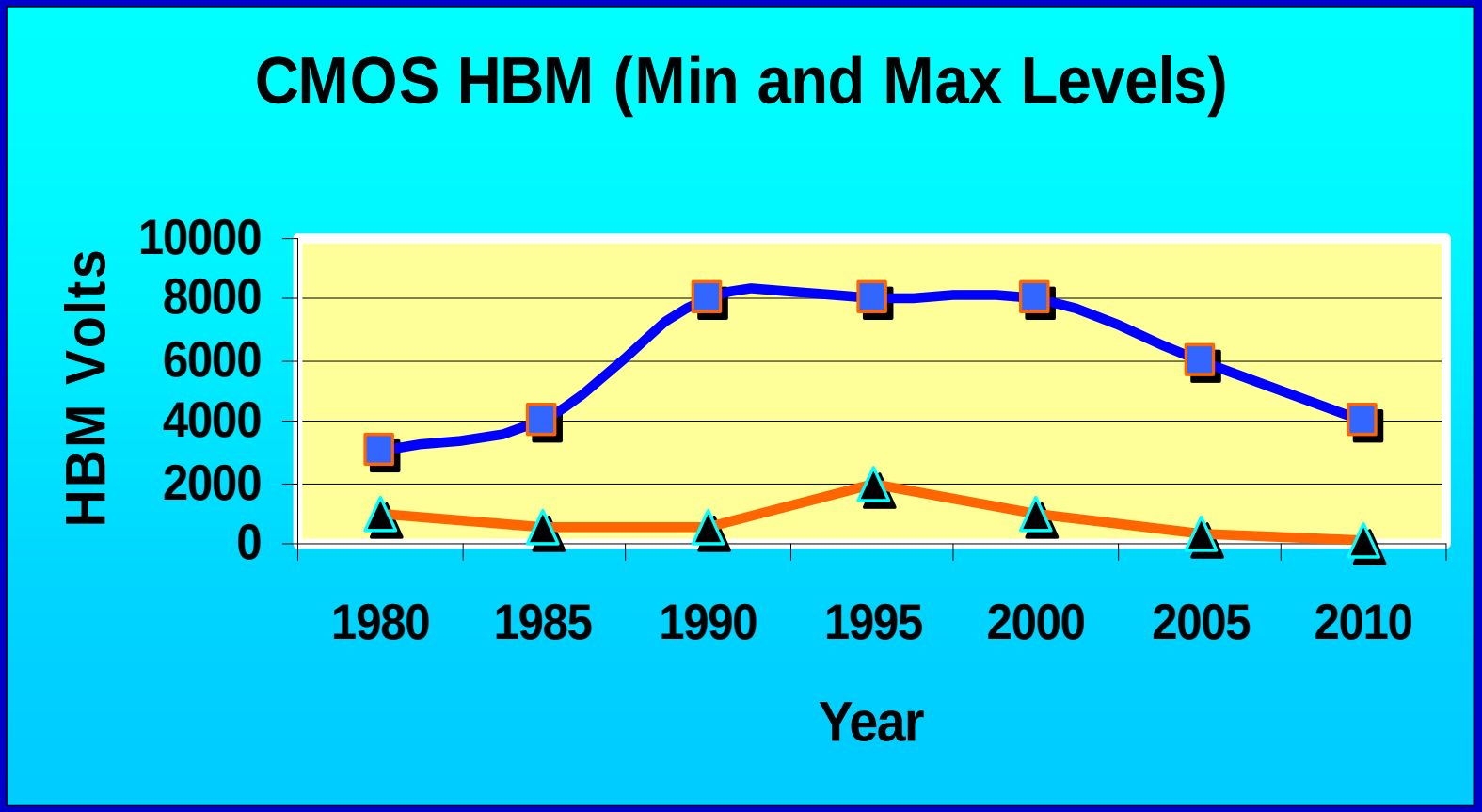


ESD: require on-chip protection

IEC: requires off-chip and on-chip protection

EOS: requires care during customer applications

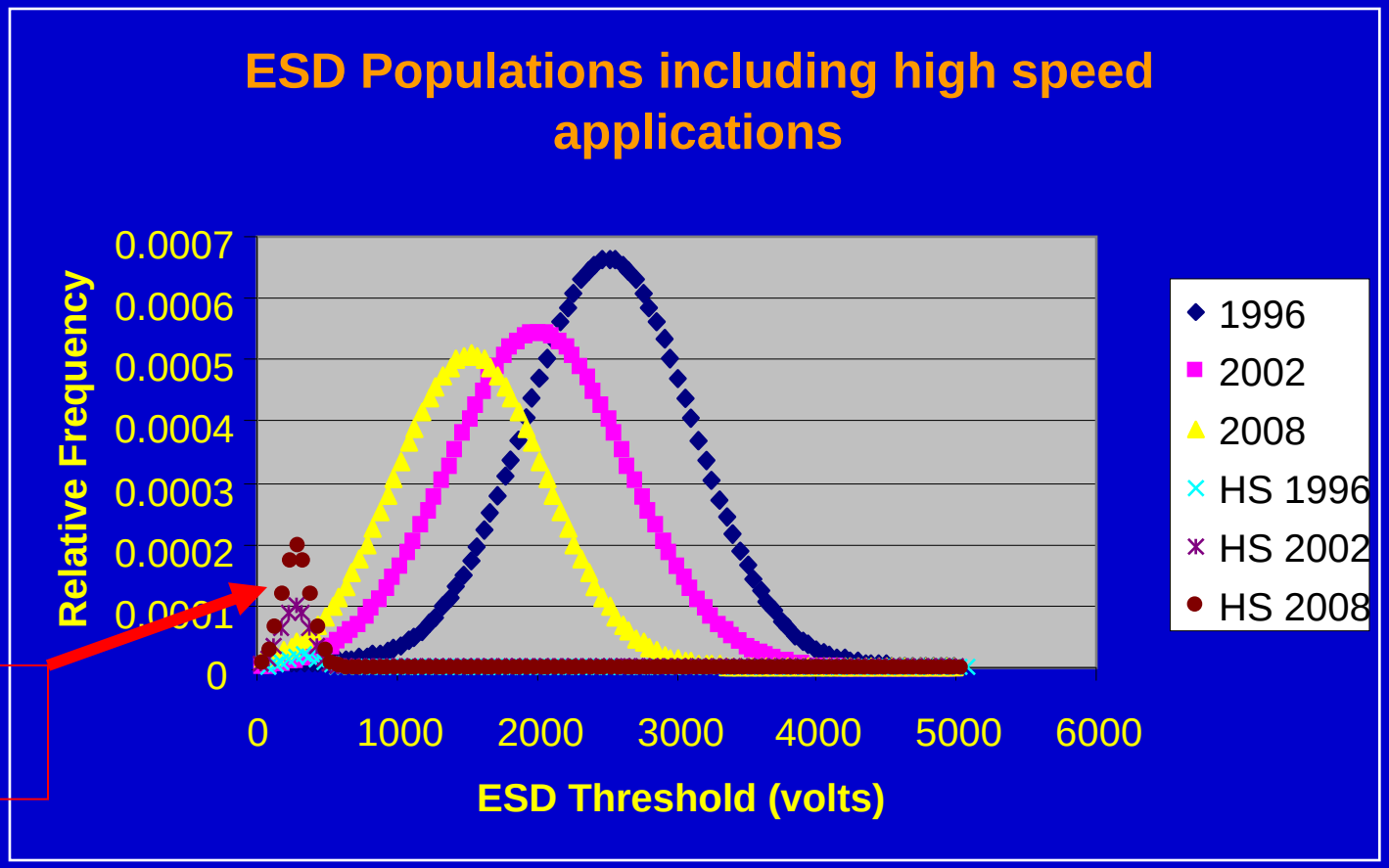
ESD Technology Road Map



A number of IC design constraints can reduce the ESD protection levels for the sensitive high speed chips will continue to degrade

ESD Threshold Population Trends

Analysis by Dr. Terry Welsher, Dangelmayer Associates

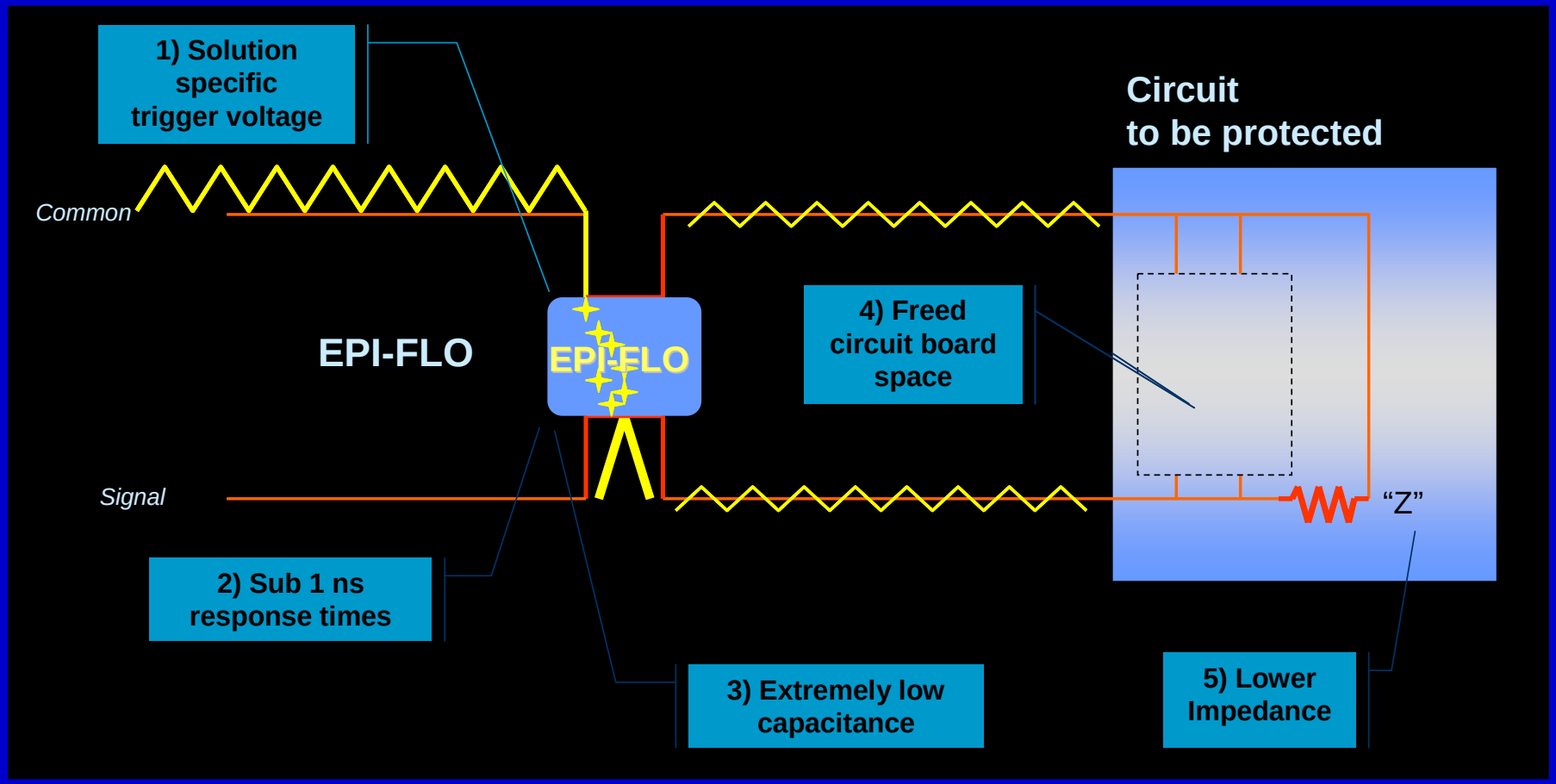


Bimodal Distribution

High Speed Population

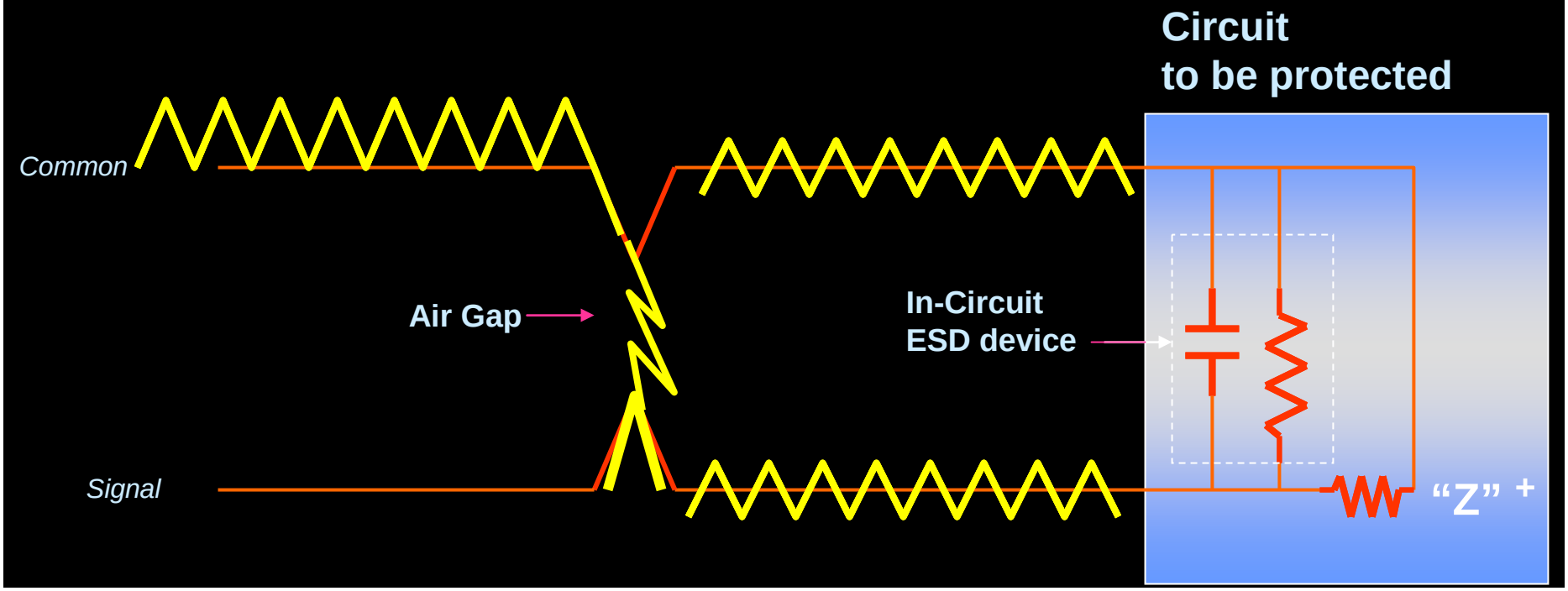
Slide Courtesy Dangelmayer Associates

New Research: Polymer Voltage Suppressors (PVS) low capacitance ESD protection increases GHz Electronics availability by increasing reliability.



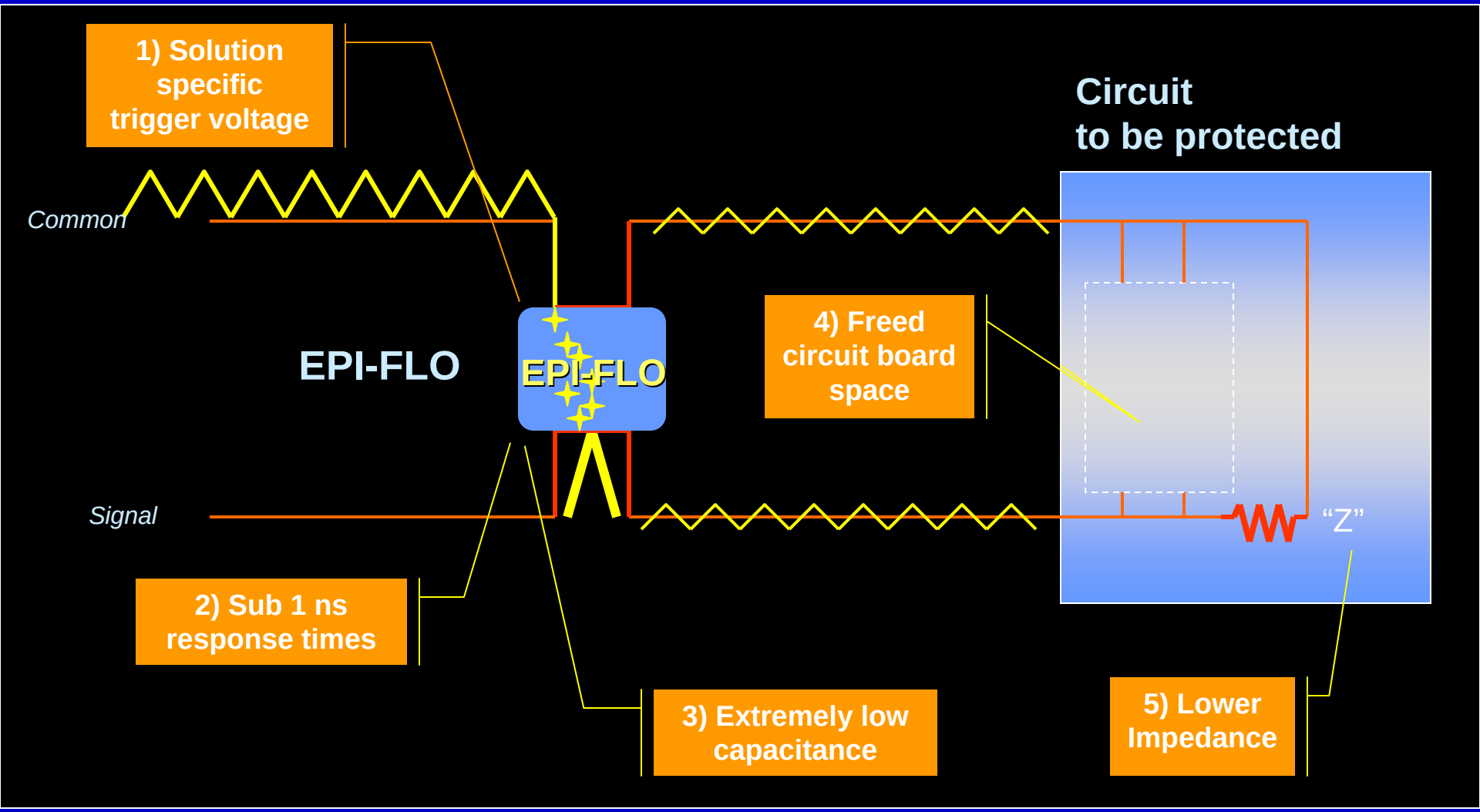
Courtesy: Electronics Polymers Inc.

Air Gap based ESD protection

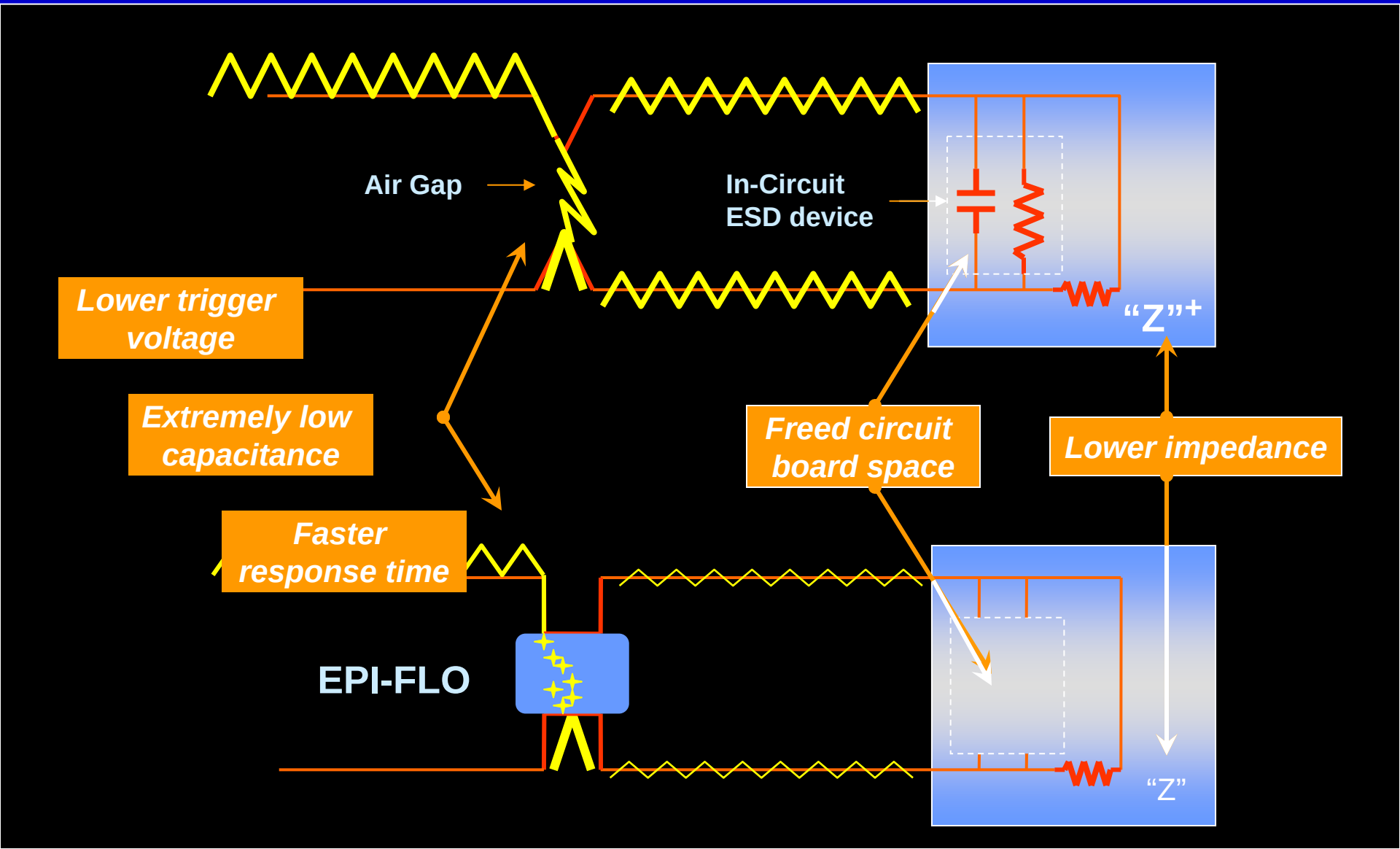


Features

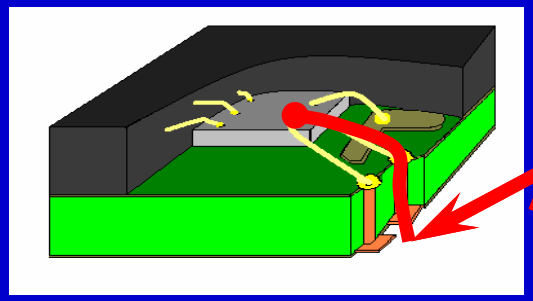
•Polymer Voltage Suppressors (PVS) can offer low capacitance ESD protection



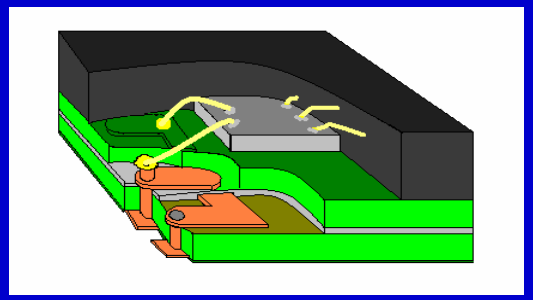
Why is this better?



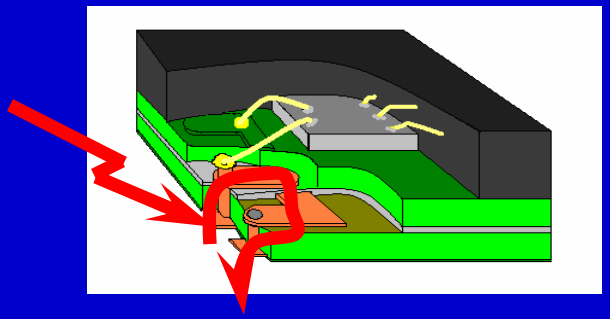
Can this polymer be integrated into IC package?



No protection Damages IC



Polymer in IC Package



Polymer ESD Protection

Summary and Outlook

- ESD is always a major concern for IC components and electronics systems that are built with these components
- Every consumer must be aware of ESD as they handle their personal electronics
- Rapid advances in technologies and circuit performance requirements are making ESD reliability into a constant challenge

Summary and Outlook

- Newer IC packages will make ESD testing even more complicated
- Integration of ESD suppressive materials into the IC package itself is one option that needs to be explored
- Package research must also address innovation towards non-exposed pins or sealed IC pins to minimize the ESD threat
- Research into ultra low capacitance package types will also be crucial for maintaining safe ESD levels for very large packages

Acknowledgments

- ESD Association (ESDA)
- More information on ESD can be obtained from www.esda.org
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- Mr. Ted Dangelmayer, Dangelmayer and Associates
- Dr. Karen Shrier, Electronics Polymers Inc.